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Fabrication of Diodes Using the Si-iBP-Si SOI Structure*

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As a step toward realizing 3-*D* integration for IC's diodes are fabricated on the Si-iBP-Si SOI structure and their electrical properties are evaluated. For the planar junction diode, the forward current is exponentially proportional to the forward voltage, $I_f \propto \exp(qV_f/nkT)$, where the value of n is 1.7~2.2 depending on the region. The reverse current is in proportion to the 1/2~1/3 power of the reverse voltage, $I_r \propto V_r^{1/2\sim1/3}$, and the reverse breakdown voltage is over |30|V. For the poly-Si gate MOS diode the average threshold voltage is about V_T=-1.5~-2V, and the measured C-V characteristic curves are almost equal to the ideal one and no hysteresis phenomena are observed.

I. INTRODUCTION

As the production techniques for IC's become more and more developed, the level of integration gradually reaches a upper limit. In order to over come this limit, many studies are being done on expanding the scope of integration from 2 dimensions to 3. Among materials for the 3-D integration, the SOI (silicon on insulator) structure is well known as the most practical and it is becoming the center of much interest. The SOI structure has many forms such as silicon on sapphire, silicon on nitride, silicon on oxide and so on. There are, however, many disadventages in growing Si on an insulator. That is to say, some additional tasks are required such as recrystallization because of the difficulty in direct Si epitaxy and also many crystalline defects appear at the Si-insulator interface due to the large differences between the lattice constants and thermal expansion coefficients of Si and Insulator.

In this study, for the solution of the above mentioned problems BP (boron monophosphide) which is an almost unknown III-V compound is proposed as the insulator for a SOI structure. It has previously been reported that single crystal BP could be grown on a Si substrate and then epitaxial Si on the BP-Si substrate despite the large difference between the lattice constants of BP (a_0=4.53Å) and Si(a_0=5.43 Å)[1,2]. In addition, it has also been known that the BP on Si becomes iBP(insulating BP) with high resistivity when heat treated[3]. Considering the above facts, the Si-iBP-Si structure should be usable as a SOI without any additional effort.

In the present study, planar junction and MOS diodes are formed on this Si-iBP-Si structure and their electrical properties are evaluated through I-V and C-V characteristic curves.

II. FORMATION OF THE Si-iBP-Si STRUCTURE

The experimental apparatus and the optimum growth conditions for the Si-BP-Si structure have previously been described[1]. First, the 0.5 μm thick single crystal BP layer is grown on an n-type

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Si(100) substrate having a resistivity of 4-8 Ωcm by the thermal reaction of B_2H_6 and PH_3 in H_2 at 950°C. An n-BP layer with $\rho = 10^{-2}\Omega cm$ is formed at this growth temperature which is consistent with the report of Takenaka et al[4]. The flow rates of reactant gases are 20 cc/min for 1% B_2H_6 in H_2, 500 cc/min for 5% PH_3 in H_2 and 2500 cc/min for the H_2 carrier gas. In this case, the average growth rate is about 500 Å/min.

In order to obtain iBP, the surface of the BP is overcoated with 500 Å of Si_3N_4 deposited by the thermal reaction of SiH_4 and NH_3 in N_2 at 800°C and the sample is heated to 1050°C for 2 hours in N_2. Then, the Si_3N_4 is etched away using hydrofluoric acid and the resistivity of the heat treated BP is measured by the four-point probe method. This confirms that the n-type BP has become iBP with a resistivity of about $10^{12}\Omega cm$. The high crystalline perfection of the iBP layer is confirmed by RED (reflection electron diffraction) and TED (transmission electron diffraction) patterns. Previous investigations have reported on the crystalline properties of the BP and Si layers through electron diffraction patterns[1,2].

Next, a 5 μm thick epitaxial Si layer is grown on the iBP-Si substrate. The optimum growth conditions for epitaxial Si are a growth temperature of 1050 ℃ and flow rates of 5% SiH_4 in the H_2 carrier gas of 30 and 3000 cc/min, respectively. Under these conditions the average growth rate of epitaxial Si is about 3500 Å/min. Though no doping gas is used during the deposition, the epitaxial Si layer has n-type conductivity. It has been reported that the n-type conductivity of the epitaxial Si layer is caused by the phosphorus atoms deposited on the inner wall of the reaction chamber[5]. The dopant concentration of the epitaxial Si layer is about $10^{15}cm^{-3}$. The high crystalline perfection of the epitaxial Si layer is also certified by the electron diffraction patterns. A cross-section of the formed Si-iBP-Si structure, on which the planar junction and MOS diodes are fabricated, is shown in Fig.1.

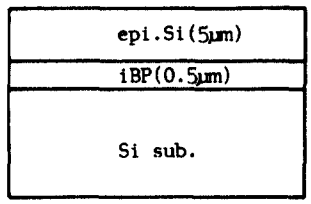

Fig. 1. Cross-section of the Si-iBP-Si structure.

III. PLANAR JUNCTION DIODE

1. Fabrication

The cross-section of the planar junction diode formed on the Si-iBP-Si structure is shown in Fig.2. First, a 2000 Å thick SiO_2 layer is formed thermally on the n-type epitaxial Si layer at 1050°C during 3 hours in dry O_2. By photolithography a 0.4x0.4 mm^2 square-shaped window is opened and a 3000Å of CVD-BN (chemical vapor deposition-boron nitride)[6] is deposited by thermal reaction between B_2H_6 and NH_3 in N_2 at 780°C. Then, the sample is put into an electrical furnace and the diffusion process allowed to proceed at 1050°C for 30 min in N_2. After that, the excess Si_3N_4 and CVD-BN are removed by HF and H_3PO_4 etching solution boiling at 160°C, respectively. The junction depth is about 2.7 μm and the surface concentration of the

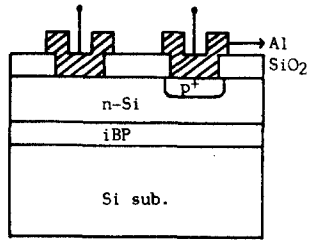

Fig. 2. Cross-section of the planar junction diode.

P-type diffusion well is about $2.3\times10^{20}cm^{-3}$. The above values are measured by the spherical drilling method and the four-point probe method respectively.

While, some phosphorus diffusion arises from the iBP layer into both the epitaxial Si layer and the Si substrate during the oxidation and diffusion processes[4], it is not very significant since the junction depth is less than 1 μm at most. The temperature for the oxidation and diffusion is fixed at 1050°C as this is the stoichiometric temperature of n-type BP[3]. Again means of photolithography another window is opened and Al electrodes are attached on the two windows by the evaporation method.

2. Electrical properties

Sah et al. reported[7] that the empirical I-V characteristic curve of the p-n junction diode deviates from the ideal one obtained by Shockley[8] due to carrier recombination and generation inside the sapce charge region. According to their model, a typical Si p-n junction diode has an apparent $\exp(qV/nkT)$ dependence for the forward current and a nonsaturable reverse current

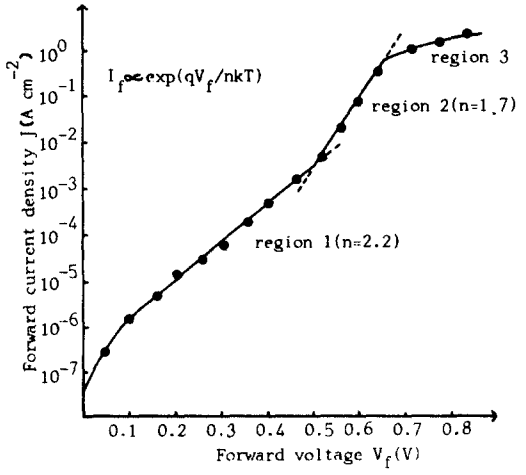

Fig. 3. Forward characteristics of the planar junction diode.

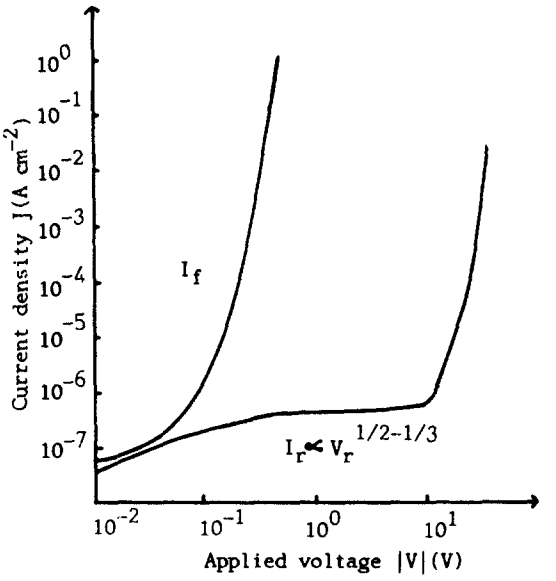

Fig. 4. Reverse characteristics of the planar junction diode.

characteristic. The measured I-V curve is shown in Fig.3. In the figure, the average value of n is about 2.2 in the recombination current region (region 1) and about 1.7 in the diffusion current region (region 2). A linear ohmic region (region 3) is also observed. Although the values of n are not exactly consistent with the experimental values obtained by Sah et al.,[7] the general shape of the forward I-V curve follows their empirical result fairly well.

The reverse characteristic of the diode is shown in Fig.4. The reverse current Ir, which is proportionate to the reverse voltage, $V_r^{1/2\sim1/3}$, originates as a recombination-generation current in the space charge region. The fabricated diode exhibits the typical junction type characteristic between the step and linear-graded junction and as supposed, the reverse current is nonsaturable. The breakdown voltage is over 30 V.

Considering the fact that the diode is formed on the SOI structure, it displays relatively good results; therefore, it is possible to fabricate a

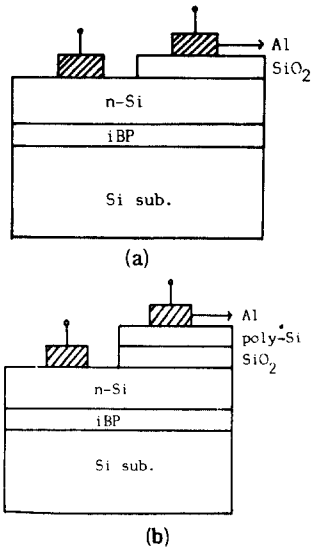

Fig. 5. Cross-sections of MOS diodes,
(a) Typical MOS diode,
(b) Poly-Si gate MOS diode.

planar junction diode having good electrical characteristic on the Si-iBP-Si SOI structure.

IV. MOS DIODES

1. Fabrication

Fig.5 shows the cross-sections of the MOS and poly-Si gate MOS diodes fabricated on the Si-iBP-Si structure. For the MOS diode, a 1000 Å thick SiO_2 layer is thermally grown on the epitaxial Si layer at 1050°C during 1 hour in dry O_2. Then, by photolithography half of the oxide layer is removed in hydrofluoric acid and Al electrodes 0.6 mm in diameter are attached to both the epitaxial Si and oxide layers by the evaporation method. For the poly-Si gate MOS diode, the 1000 Å thick SiO_2 layer is grown thermally on the epitaxial Si layer under the same conditions as above and subsequently n-type poly-Si is deposited by the pyrolysis of SiH_4 with PH_3 at 800°C in H_2. After that, by photolithography half of both the poly-Si and SiO_2 layers are removed by a HF-HNO_3 mixture and a HF solution respectively and Al electrodes 0.6 mm in diameter are attached to the epitaxial Si and poly-Si layers. The resistivity of the n-type poly-Si layer measured by the four-point probe method is about 1.5×10^{-4} Ω cm.

2. Electrical properties

Fig.6 shows C-V curves and a distribution chart of the threshold voltage V_t for the MOS diodes. The empirical C-V curves are compared with the ideal one obtained by Goetzberger[9]. Two samples of the MOS diode were measured for the C-V curves. The measured flat band voltage V_{fb} of the two samples deviates from the ideal by 1~2V, but the variation of minimum capacitance C_{min} and maximum capacitance C_{max} is negligible. For instance, C_{fb}/C_{max} is about 0.7, where C_{fb} is the flat band capacitance, and C_{min}/C_{max} about 0.3 in all cases and the change in flat band voltage $\triangle V_{FB}$ is about 0.5 and 1.2V in the two samples. The hysteresis

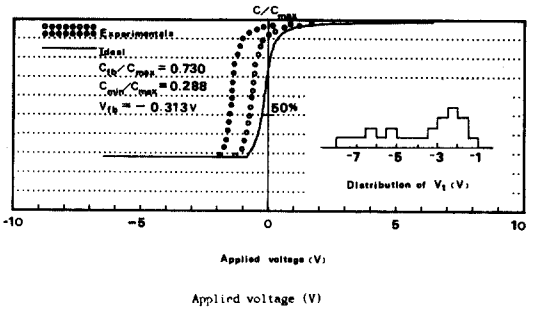

Fig. 6. Characteristics of typical MOS diodes.

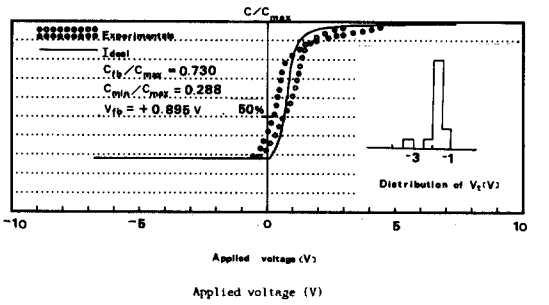

Fig. 7. Characteristics of poly-Si gate MOS diodes.

phenomena which result from hole traps at the $Si-SiO_2$ interface are not observed. Considering the distribution of V_t, the samples having V_t =-2.0 ~2.5V are most numerous, but the values of V_t are very dispersed.

In the case of the poly-Si gate MOS diodes, the C-V curves and the distribution chart of V_t are shown in Fig.7. The shift of the empirical C-V curves from the ideal one is much smaller than for the MOS diodes. The values of C_{min} and C_{max} are the same as that of the MOS diode and also unchangeable. V_{fb} has changed less than 0.5V, that is, $\triangle V_{fb}$ is about 0.1V for one and 0.3V for the other sample. Of course, no hysteresis phenomena appear and the values of V_t are strongly concentrated around -1.5~2V.

As a result, we known that the poly-Si gate MOS diode has better electrical properties than the MOS diode and in both cases the Si-iBP-Si structure can be used as a SOI for the fabrication of the MOS diodes.

V. CONCLUSIONS

In an application of the SOI structure, planar junction and MOS diodes were formed on the Si-iBP-Si structure. In case of the planar junction diode, a forward characteristic of $I_f \propto \exp(qV_f/nkT)$ was obtained, where n has a value of 1.7 ~ 2.2 depending upon the region, I_f is the forward current and V_f the forward voltage. The reverse characteristic showed a relation between the reverse current and voltage of $I_r \propto V_r^{1/2\sim1/3}$. This measured characteristic is almost consistent with the empirical result obtained by Sah et al.[7] Among the MOS diodes formed on the Si-iBP-Si structure, the poly-Si gate MOS diode displayed a good C-V characteristic curve which was more silimar to the ideal one obtained by Goetzberger[9] than that of the typical MOS diode. The poly-Si gate MOS diode had a threshold voltage of V_t = -1.5~ -2V and a change in the flat band voltage of $\triangle V_{fb} \leq 0.5$V. No hysteresis phenomena appeared in the C-V curves.

In the view of the results so far derived, we now known that the Si-iBP-Si structure can be used as a SOI structure in fabricating some diodes and more advanced devices, such as BJT, MOS FET.

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SOI로서 Si-iBP-Si 구조를 이용한 diode의 제작

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기본적인 3차원 집적화의 실현을 위해 SOI 구조인 Si-iBP-Si 구조상에 diode를 제작하였고 그 전기적인 특성을 평가하였다. 평면접합 diode의 경우, 순방향전압에 지수적으로 비례하였다. 즉 $I_f \propto \exp(qV_f/nkT)$ 로 n은 각 영역에 따라 1.7~2.2의 값을 가졌다. 역방향전류는 역방향전압에 $I_r \propto V_r^{1/2\sim1/3}$의 형태로 비례하였고, 역방향항복전압은 |30|V 이상이었다. poly-Si을 gate로 한 MOS diode의 경우, 문턱전압의 평균치는 $V_T = -1.5 \sim -2$V로 나타났으며 측정된 C-V 특성곡선은 이상곡선에 거의 일치하였고 hysteresis 현상은 관찰되지 않았다.