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Organic thin film transistors with polyvinyl alcohol treated dielectric surface

Jung Hoon Seo[1], Jae-Hong Kwon[1], Sang-Il Shin[1], Kyung-Soo Suh[2] and Byeong-Kwon Ju[1]

[1] Display and Nanosystem Laboratory, College of Engineering, Korea University, Anam-dong, Seongbuk-gu, Seoul 136-701, Korea
[2] Convergence and Components Laboratory (ICCL), Electronics and Telecommunications Research Institute (ETRI), Daejeon 305-700, Korea

E-mail: bkju@korea.ac.kr

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Abstract
This is a report on a simple method for improving poly-4-vinylphenol (PVP) organic thin-film transistors (OTFTs). To decrease surface roughness so that we could form a larger grain size, we coated a polyvinyl alcohol (PVA) film onto the PVP dielectric layer. The effect of PVA treated gate dielectric surface modification has been examined and these organic transistors showed improved electrical characteristics with field effect mobility of 3.6×10^{-2} cm^2 V^{-1} s^{-1} and a I_{on}/I_{off} ratio of 2.11×10^5. The results demonstrate the possibility of a simple enhancement method through the process which uses a polymer thin film.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Organic thin-film transistors (OTFTs) have been considered as a promising technology for flexible electronics because of their unique advantages such as their flexibility, light weight and low-cost fabrication. With these characteristics, OTFTs can be adapted to many applications such as active matrix liquid crystal displays [1, 2], radiofrequency identification (RFID) tags [3] and chemical sensors [4]. The performance of OTFTs on non-planar and rigid substrates, such as glass or plastic, has been inferior to that of poly-Si TFTs or amorphous-Si TFTs on Si wafers [5]. In order to make OTFTs operate at a low voltage with high mobility, it is very important to improve either the materials of the dielectric layer or the active layer and device structure. Many researchers have studied unique treatments such as coating a self-assembled monolayer (SAM) layer onto the gate dielectric layer, mixing high-K particles in the conventional dielectric materials, and forming organic–inorganic combined dielectric layers in order to enhance the overall device performance. In the case of the surface treatment method, Kim *et al* in 2004 reported a SAM layer on the zirconium oxide (ZrO_2) dielectric layer with octadecyltrimethoxysilane (OTMS) [6]. Song in 2002 reported hexamethyldisilazane (HMDS), and octadecyltrichlorosilane (OTS) treatment on the SiO_2 dielectric layer [7]. Through this method, the mobility increased to about five to seven times higher than that of reference devices. In the case of mixing high-K particles in the conventional dielectric materials, Lim *et al* in 2005 proposed dispersing barium titanate ($BaTiO_3$) in the PVA solution [8], Maliakal *et al* in 2005 proposed titanium dioxide (TiO_2) nanoparticles in the polystyrene (PS) dielectric polymer [9]. Through this method, the mobility increased from twice to five times higher than that of the reference device. The case of forming organic–inorganic combined dielectric layers, poly-4-vinylphenol (PVP)/cerium dioxide–silicon dioxide (CeO_2–SiO_2) composite double gate dielectrics on the indium–tin oxide (ITO) substrate were described in the work of S Kim *et al* in 2006 [10]. Through this method, device mobility improved twice compared to that of the reference device. These unique methods, however, had disadvantages. For example, the SAM layer is weak for an aceton-group solution when patterning. Other inorganic-related methods are quite expensive or involve a complicated procedure to form an inorganic dielectric layer or inorganic particles for the dielectric layer. Moreover, it is hard to have flexibility when an inorganic layer is inserted. For this reason, it is necessary to improve device performance using a soluble material. Here, we describe organic thin-film transistors with polyvinyl alcohol (PVA) that acts as a

passivation layer to enhance dielectric properties and grain growth of pentacene so that there is a beneficial improvement for the overall device parameters. In this paper, we present our analysis of the dielectric constant change per frequency variation, fabrication process, and surface morphology after PVA polymer passivation and electrical characteristics in order to better understand its possibilities if used as a dielectric layer.

2. Experimental details

2.1. The synthesis of dielectric materials

To form a PVP thin film, PVP powder (Aldrich Company, Mw ∼20 000) was mixed with 13 wt% of propylene glycol monomethyl ether acetate (PGMEA, Aldrich Company), and poly melamine-co-formaldehyde methylated (Aldrich Company, Mn ∼511) was then added to the PVP solution at a ratio of 1:20. PVA powder (Aldrich Company, Mw ∼30 000–70 000) was mixed with a cross-linking agent, i.e. ammonium bicarbonate powder (Aldrich), at a ratio of 5:1, and was dissolved in water at a concentration of 1 wt%.

2.2. Device fabrication

In the fabrication procedure, the double side polished glass substrate was first cleaned using acetone, methanol and deionized (DI) water using an ultrasonic cleaner (Daihan Scientific Co., Ltd; 50 W, 45 kHz). First, 200 nm thick Al, serving as the gate electrode, was deposited using a thermal evaporation technique at a deposition rate of 4–5 Å s^{-1} using a shadow mask. The PVP dielectric layer was formed by spin coating and cross-linking at 200 °C for 5 min on a hotplate to enforce the polymer. After fabricating the PVP thin film, the PVA solution was coated on it. The PVA thin film was coated by a spin coater and cross linked using ultraviolet radiation ($\lambda \sim 365$ nm). The average final thickness of the PVA/PVP double layer films was measured as 370 nm (30 nm of PVA and 340 nm of PVP) by a surface profiler (Dektak 3030 profilometer). Pentacene was deposited using a thermal evaporator at a deposition rate of 0.7 Å s^{-1} using a shadow mask (Dov Co., Ltd). The final thickness was 60 nm. 250 nm thick Au that served as the source/drain (S/D) electrodes were thermally deposited at 4–5 Å s^{-1} using a shadow mask. These OTFTs were the top contact devices with a channel width of 1000 μm and length of 100 μm fabricated using the mask alignable thermal evaporator system.

2.3. Measurements

The current–voltage (*I–V*) characteristics of these OTFTs were measured by two Keithley 237 source-measure units and the capacitance–frequency (*C–F*) characteristics were measured by a Keithley 590 *C–V* analyzer and HP-4192 Impedance Analyzer. The surface condition was characterized by an atomic force microscope (AFM) by Digital Instruments Nanoscope III.

3. Results and discussion

In order to measure the capacitance versus frequency relationship, we fabricated two metal–insulator–semiconductor (MIS) structures. We used the same MIS structures but the difference was that MIS 1 had PVP while MIS 2 had a PVA treated PVP dielectric layer (PVA/PVP layer). Figure 1 shows the *C–F* (capacitance–frequency) characteristic from 100 Hz to 10 MHz with a capacitor area of 0.0025 cm^2. The MIS 1 showed a steep reduction tendency of capacitance at high frequency (over at 1 MHz); however the MIS 2 device, treated by the PVA film, tended to reduce gradually at the same frequency. When capacitance (C_P) is expressed as a function of the frequency f, the dielectric properties usually change by a frequency. In this paper we assumed a non-ideal capacitor with parallel capacitance and resistance. The capacitance expressed correlation between

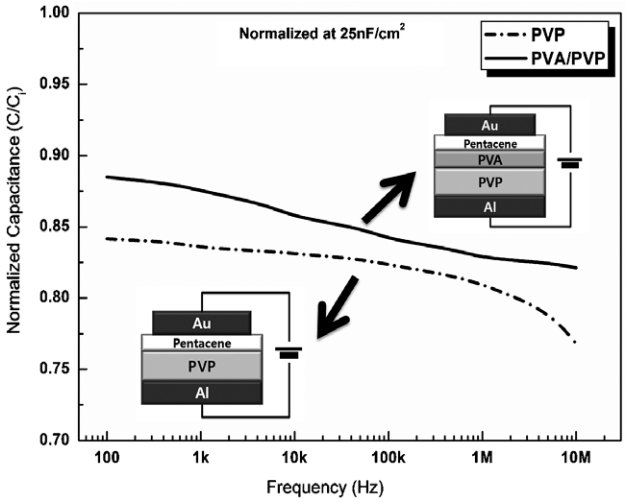

Figure 1. Normalized capacitance of the MIS device (Au/Pentacene/polymer insulator material/Al) at 25 nF cm^{-2} versus frequency from 100 Hz to 10 MHz. In this work, we measured the MIS devices with PVP and PVA treated PVP thin film.

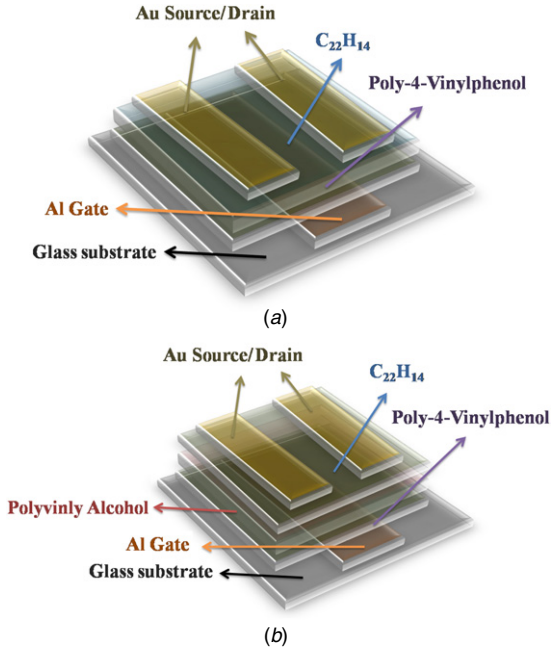

Figure 2. (*a*) Schematic diagrams of OTFTs with a PVP insulator layer, and (*b*) the PVP coated by the PVA film.

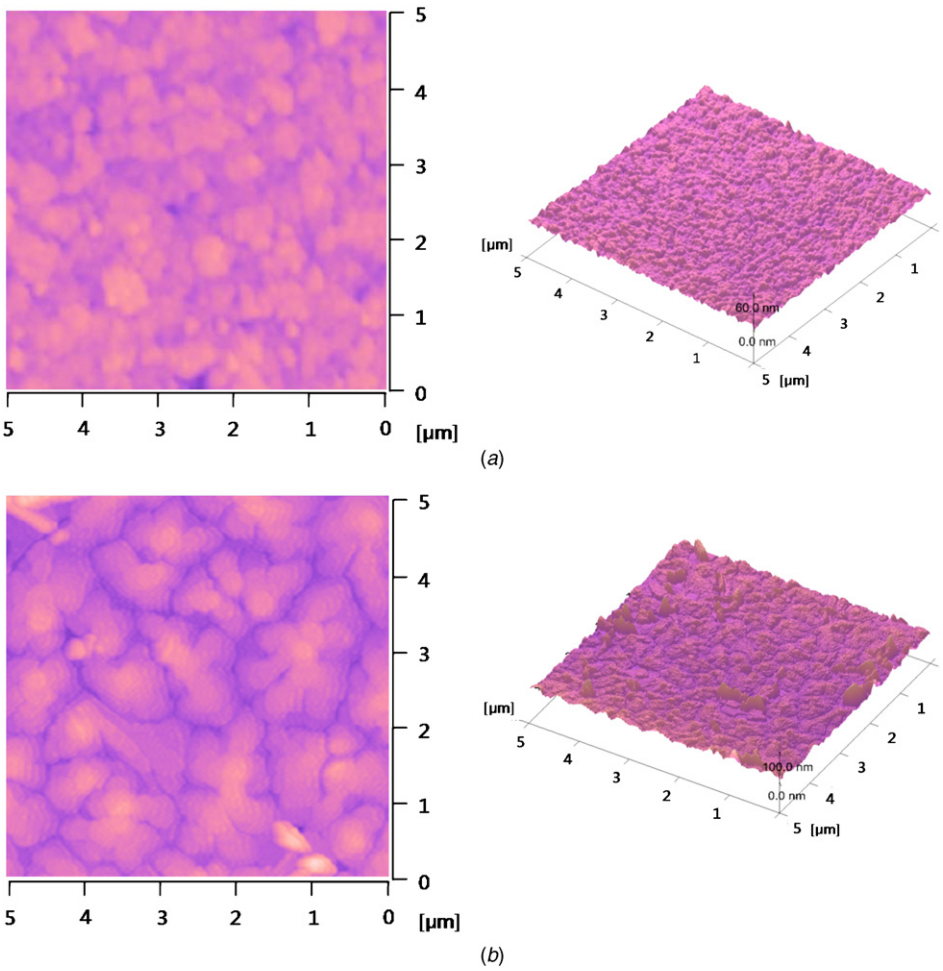

Figure 3. Atomic force microscopy (AFM) images of pentacene deposited onto (*a*) a PVP-dielectric layer without a PVA film coating and (*b*) with a PVA film coating. The pentacene layer has an average thickness of 60 nm. The average grain size and RMS roughness changed from 400 nm to 1500 nm and 4.94 nm to 2.69 nm, respectively.

Table 1. A tabulation of dielectric constant, capacitance per unit area, threshold voltage (V_{th}), sub-threshold slope (S), off-state current (A), on-state current (A), field effect mobility (μ) and I_{on}/I_{off} ratio for PVP-OTFTs and PVA coated PVP-OTFTs.

	Dielectric constant (ε_r)	Capacitance (nF cm^{-2})	Threshold voltage (V)	Subthreshold slope (V/decade)	Off-state current (A)	On-state current (A)	Mobility (cm^2 V^{-1} s^{-1})	On/off ratio
PVP OTFT	4.05	19.94	−4.1	2.95	-1.55×10^{-10}	-6.39×10^{-6}	0.023	4.12×10^4
PVA-PVP OTFT	8.58	20.36	−2.9	1.72	-4.29×10^{-11}	-9.07×10^{-6}	0.036	2.11×10^5

the ideal capacitance and the impedance Xc is given by equation (1),

$$X_C = \frac{1}{\mathrm{i} \cdot \omega \cdot C_P}. \tag{1}$$

In order to calculate losses due to leakage, the impedance Z for a real capacitor is more complex and given by equation (2):

$$\begin{aligned} Y &= \frac{1}{Z} = \frac{1}{R_P} + \frac{1}{X_C} \\ &= \frac{1}{R_P} + \mathrm{i} \cdot \omega \cdot C_P = \frac{1}{R_P} + \mathrm{i} \cdot \omega \cdot (C' - \mathrm{i}C'') \\ &= \frac{1}{R_P} + \omega \cdot C'' + \mathrm{i} \cdot \omega \cdot C' = G + \mathrm{i}B. \end{aligned} \tag{2}$$

The admittance Y is expressed with the conductance G as a real part and the susceptance $\mathrm{i}B$ as an imaginary part. So tangent loss D or $\tan(\delta)$ is defined as equation (3):

$$D = \tan(\delta) = \frac{G}{B} = \frac{\frac{1}{R_P} + \omega \cdot C''}{\omega \cdot C'} = \frac{1}{R_P \cdot \omega \cdot C'} + \frac{C''}{C'}. \tag{3}$$

The last term (the imaginary part of the capacitance C'' divided by the real part of the capacitance C') describes the ratio of the energy lost per cycle to the energy stored per cycle, while the prefactor contributes to frequency dependence ($\omega = 2\pi f$). In the case of low resistances Rp or high frequencies, the prefactor becomes dominant. The PVA treated MIS device, thus, effectively prevents capacitance loss by the leakage resistance factor compared with the non-treated MIS device as shown in figure 1 at a high-frequency regime where the prefactor is dominant. The dielectric constant was also changed when we passivated the PVP dielectric layer. We calculated the

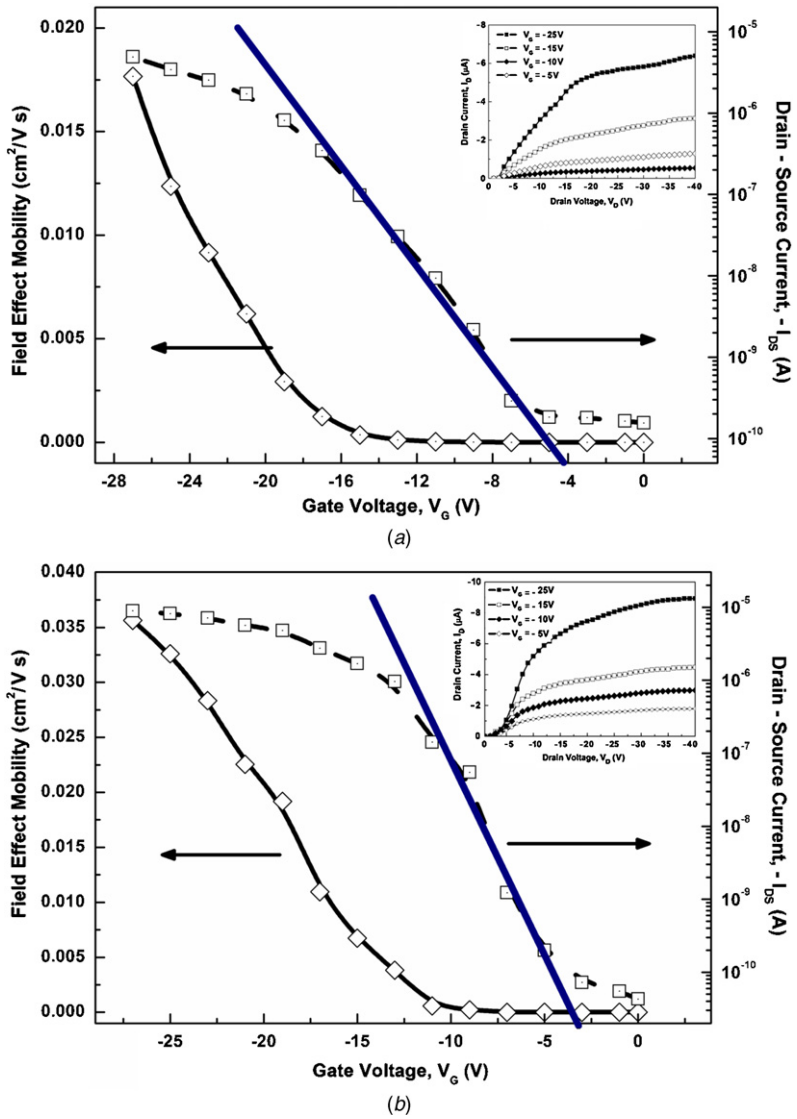

Figure 4. A plot of the drain current (I_D) versus the drain voltage (V_D) with gate voltage (V_G) from 5 to 25 V. The insets show the transfer characteristics of the devices with mobility versus V_G and $\log_{10}$ (I_D) versus V_G for the OTFTs: (*a*) the PVP-OTFT without the PVA film coating and (*b*) with the PVA film coating. A mobility of 2.3×10^{-2} cm^2 V^{-1} s^{-1} and a I_{on}/I_{off} ratio of 4.12×10^4 were measured for the PVP-OTFTs, while a mobility of 3.6×10^{-2} cm^2 V^{-1} s^{-1} and a I_{on}/I_{off} ratio of 2.11×10^5 were measured for the PVA coated PVP-OTFTs.

dielectric constant by $C = \varepsilon_0 \varepsilon_r A/t$, where C is the capacitance per unit area, ε_0 is the free space permittivity, A is the area of the capacitor and t is the thickness of dielectric layers. For a PVP film with a cross-linking agent, the dielectric constant is 4.05 at 1 MHz and the capacitance per unit area is 19.94 nF cm^{-2}. After inserting a 30 nm PVA film, the dielectric constant and the capacitance per unit area increased up to 8.58 and 20.36 nF cm^{-2}, respectively. Based on the following equation, $1/C_{tot} = 1/C_{PVA} + 1/C_{PVP}$, the capacitance of the PVA/PVP layer worked out to be 18.36 nF cm^{-2}, because the capacitances were series connected. The theoretical capacitance value is somewhat different from our experimental result (20.36 nF cm^{-2}). We cannot clearly explain the cause of this difference but this result may be related to the trapping of carriers at defect sites in the polymer dielectric film or the carrier localization between the PVP and the PVA film which remained from the cross-linking agent or the interface of the PVP and PVA film.

AFM measurements were carried out in order to investigate the morphology of the pentacene layer in the channel. As can be seen in figure 3, there was a relevant difference in the morphology of the pentacene film deposited. When we investigated the pentacene layer on the PVA film which was coated on the PVP dielectric layer, the average grain size increased from 400 nm to 1500 nm. Since the surface morphography changed, after the PVA film was coated, from RMS roughness of 4.94 nm to 2.69 nm, the larger grains on these OTFTs indicated the smaller surface energy of the gate dielectrics and this disturbed the crystallization of pentacene.

Figures 4(*a*) and (*b*) show the drain current–drain voltage curves (I_D–V_D), the field effect mobility–gate voltage ($\mu \sim V_G$) and the $\log_{10}$ drain current–gate voltage (I_D–V_G) obtained from our OTFTs with a gate dielectric layer of the PVP and PVA/PVP layers as shown in figure 2. The source drain width and length were 1000 μm and 100 μm, respectively. In order to measure reference data, the drain current was measured based

on the Al/PVP/Pentacene/Au structure OTFTs of maximum saturation drain current of 6.45 μA under a gate voltage (V_G) of −30 V and drain voltage (V_D) from 0 to −40 V. The output current of the OTFTs with the PVA/PVP layer was reached at 9.07 μA at −30 V of gate voltage and 0 to −40 V drain voltage (V_D). The threshold voltages of the PVP OTFTs and PVA film coated PVP-OTFTs were achieved to −4.1 V and −2.9 V. Under a given gate voltage (V_G), the device with the PVA/PVP layer showed higher drain–source current and better saturation behavior as compared with using the PVP as a dielectric layer:

$$I_{DS} = \frac{1}{2}\mu_{eff} C_{PAP+PVA}\left(\frac{W}{L}\right)(V_G - V_T)^2 . \quad (4)$$

Using equation (4), we calculated the maximum hole mobility, where $C_{PVA/PVP}$ is the capacitance per unit area of the PVA/PVP dielectric layer and V_T is the threshold voltage. The OTFTs fabricated with the PVA/PVP layer had a higher field effect hole mobility of 3.6×10^{-2} cm^2 V^{-1} s^{-1} than the device with the single PVP dielectric layer, which also appeared to have relatively good mobility of 2.3×10^{-2} cm^2 V^{-1} s^{-1} at V_G of −30 V. The electric parameters are summarized in table 1. As you see from table 1, we found that there was a one order of magnitude difference of the off-state current (-1.55×10^{-10} (PVP-OTFTs), -4.29×10^{-11} (PVA/PVP-OTFTs)). As the off-state current has a major relationship with the leakage current of the insulator layer, this result might be caused by the higher dielectric constant of the PVA/PVP layer. Furthermore, we calculated the inverse sub-threshold slope S given by equation (5):

$$S = \left[\frac{\mathrm{d}\,\log(I_d)}{\mathrm{d}V_g}\right]^{-1} . \quad (5)$$

We obtained $S = 1.72$ V dec^{-1} and $S = 2.95$ V dec^{-1} for the PVA coating OTFTs and non-PVA coating OTFTs devices, respectively. Due to the subthreshold swing that shows the trap behavior and the interface quality between the dielectric layer and active layer [11], the maximum interface trap density is given by assuming that densities of the interface states are independent of energy [12, 13]:

$$N_{SS} = \left[\frac{S \cdot \log(e)}{kT/q} - 1\right]\frac{c_i}{q} . \quad (6)$$

Substituting PVP-OTFTs with $C_i = 19.94$ nf cm^{-2} and $S = 2.95$ V/decade yields an approximate interface trap density of 6.0×10^{12} cm^{-2} eV^{-1}. However, our PVA/PVP-OTFTs with $C_i = 20.36$ nf cm^{-2} and $S = 1.72$ V/decade show 3.5×10^{12} cm^{-2} eV^{-1} of interface trap density and this value is almost half of the trap density compared to non-PVA treated OTFTs. From these results, thus, we can explain that when we treated the PVA on the PVP dielectric layer, this has an effect on not only decreasing the interface trap density but also lowering the subthreshold swing. As a result, to coat the PVA film onto the PVP layer attributes to the growth of the grain size and to the lowering of the surface roughness so that it affects overall device performance. Thus, the method we propose in this work is considered as a simple but highly useful method to improve device characteristics.

4. Summary

OTFTs with a PVA film coating were fabricated. The use of the PVA film affected the capacitance per unit area from 19.94 nF cm^{-2} to 20.36 nF cm^{-2} and the dielectric constant from $\varepsilon_r = 4.05$ to $\varepsilon_r = 8.58$, respectively. Moreover, shown as a *C–F* result with the MIS device, we found that the phenomenon where the capacitance property was over 1 MHz of frequency would not drastically drop. We also observed the larger grain size of the active layer so that we achieved a lower operation voltage from −4.1 V to −2.9 V and approximately twice the improvement for the on/off ratio and mobility. This value is somehow a low value as compared to another surface treatment method mentioned in the introduction to this paper. However, the PVA film could coat easily and resist an aceton group solution. We, therefore, strongly believe that our PVA coating method placed onto the PVP dielectric layer is a promising gate dielectric structure for high performance OTFTs.

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References

[1] Sheats J R 2004 *J. Mater. Res.* **19** 1974
[2] Nomoto K, Hirai N, Yoneya N, Kawashima N, Noda M, Wada M and Kasahara J 2005 *IEEE Trans. Electron Devices* **52** 1519
[3] Kelley T W, Baude P F, Gerlach C, Ender D F, Muyres D, Haase M A, Vogel D E and Theiss S D 2004 *Chem. Mater.* **16** 4413
[4] Someya T, Sekitani T, Iba S, Kato Y, Kawaguchi H and Sakurai T 2004 *Proc. Natl Acad. Sci.* **101** 9966
Comiskey B, Albert J D, Yshizawa H and Jacobson J 1998 *Nature* **394** 253
[5] Jang J and Han S H 2006 *Curr. Appl. Phys.* **6** e17
[6] Kim J M, Lee J-W, Kim J K and Ju B K 2004 *Appl. Phys. Lett.* **85** 6368
[7] Song S K 2002 *J. Electr. Eng. Tech.* **C 12C-2** 136
[8] Raoul S, Leszek A M and Martin G 2005 *Adv. Mater.* **17** 1535
[9] Maliakal A, Katz H, Cotts P M, Subramoney S and Mirau P 2005 *J. Am. Chem. Soc.* **127** 14655
[10] Kim C S, Jo S J, Lee S W, Kim W J, Baik H K, Lee S J, Hwang D K and Im S 2006 *Semicond. Sci. Technol.* **21** 1022
[11] Christopher R N, Frisbie C D, da Silva Filho D A, Bredas J L, Paul C E and Kent R M 2004 *Chem. Mater.* **16** 4436
[12] Rolland A, Richard J, Kleider J-P and Mencaraglia D 1993 *J. Electrochem. Soc.* **140** 3679
[13] Unni K N N, Sylvie D S and Nunzi J M 2005 *J. Phys. D: Appl. Phys.* **38** 1148