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Low temperature epoxy bonding for wafer level MEMS packaging

Yong-Kook Kim^a, Eun-Kyung Kim^b, Soo-Won Kim^a, Byeong-Kwon Ju^{c,*}

^a Department of Electronics and Computer Engineering, Korea University, Seongbuk-Gu, Seoul, 136-701, Republic of Korea ^b Department of Nano-IT Engineering, Seoul National University of Technology, Nowon-Gu, Seoul, 139-743, Republic of Korea

^c Display and Nanosystem Lab., College of Engineering, Korea University, Seongbuk-Gu, Seoul, 136-701, Republic of Korea

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Abstract

In this paper, we report on a technology for wafer-level MEMS packaging with vertical via holes and low temperature bonding using a patternable B stage epoxy. We fabricated via holes for vertical feed-throughs and then applied bottom-up copper electroplating to fill the via holes. For low temperature wafer level packaging, we used B-stage epoxy bonding in the sealing line. The optimal bonding parameters were 150 °C and 30 min. The tensile strength was about 15 MPa. Therefore, this packaging technology can be used for low temperature wafer level packaging for many MEMS devices.

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1. Introduction

For integration of MEMS chips to produce cheaper and better quality components, micro-electromechanical systems (MEMS) technology has been introduced in switches, resonators, sensors, and capacitors. Therefore, the demands for efficient packaging of these MEMS-based components have been increasing, as well. MEMS packaging is much more expensive, heavy, and large than in the case of integrated circuits' packaging. This packaging often reaches to more than 70% of the total cost of the microsystem [1,2]. Also, MEMS packaging has to be able to protect the MEMS devices from damaging environmental factors such as shock, moisture, and dust, because MEMS devices generally consist of 3D structures such as membranes, cantilevers and bridges. Efficient package of such intricate MEMS devices at a reasonable cost has been one of the critical issues in the development of commercial MEMS products [3,4]. The driving force behind MEMS packaging has not been only reduced size and weight, but primarily the fact that wafer-level packaging (WLP) technology has the potential to improve electrical performance at a comparable or even reduced manufacturing cost, thus providing an improved performance-to-price ratio. To

* Corresponding author. E-mail address: bkju@korea.ac.kr (B.-K. Ju).

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effectively reduce the package distance as well as size, highdensity and vertical interconnections have become one of the solutions. Vertical interconnections not only shrink the package area by changing the traditional two-dimensional method into a three-dimensional one, but also reduce the interconnection distance from several millimeters into hundreds of micrometers and provide smaller interconnect lengths which give lower electrical parasitic effects and smaller propagation delays [5].

A bonding technique has to provide a relatively strong bond at the lowest possible temperature. Higher temperature may damage metallization layers and cause considerable stress in the bonded materials. Adhesive wafer bonding possesses some advantages over other established bonding techniques, like anodic or direct bonding. Typical adhesive bonding has a low temperature processing range, making it fully integrated circuit (IC) compatible. Many spin-coated amorphous polymers such as polyimides, benzocyclobutene (BCB), Nafion and photoresists have been investigated as intermediate layers for wafer bonding [6–12]. Although intermediate layer bonding can be obtained at a relatively low temperature, bond strength is high and there is no limitation for the substrate material. This bonding has some disadvantages. The solvent release and polymer curing process often generate voids resulting in non-uniform bonding. The polymer bonding does not lead to a hermetic seal.

In this research, we have proposed a wafer-level packaging method with vertical via holes and low temperature bonding



Fig. 1. A schematic diagram of the proposed packaging structure.

using a patternable B stage epoxy. B-stage epoxy is an intermediate state in the reaction of a thermosetting resin where the adhesive softens when heated at a low temperature $(110-125 \degree C)$ for a brief time period (minutes) and is non-tacky when cooled to room temperature. This proposed packaging has many advantages as follow: First, costs can be reduced because this method provides wafer-level packaging. Second, the format of a vertical electric path can provide low loss electrical connections. Third, a low temperature process is achieved because there are some MEMS devices which are broken at a temperature of 150 °C. The vertical feed-through structure has many potential advantages such as high interconnection density and low resistance, capacitance, and inductance. These kinds of advantages are critical in high frequency applications. We have demonstrated waferlevel packaging with the ability to achieve good throughput using non-conductive B-stage epoxy (RP-598-2, Ablestik Co.). This method provides a simple process, easy assembly, and low temperature processing.

2. Experimental procedures

A simplified schematic diagram of the proposed packaging structure is shown in Fig. 1. This structure represents the packaging of MEMS devices using vertical copper feed-throughs and a B-stage epoxy sealing line. First, the via holes were fabricated by a deep reactive ion etching (DRIE) process and then were filled with copper by electroplating to produce high electric conductivity and low thermal stress. After gold bumps were fabricated with a thick photoresist(AZ9260) mold, non-conductive B-stage epoxy was used for perimeter sealing. This package was designed to protect devices from moisture and to transmit signals without losses.

Fig. 2 shows a flow chart of the packaging process. A highly resistive silicon (HRS > 15000 Ω m) wafer was used to reduce the substrate losses (Fig. 2(a)). Via holes were fabricated using the inductively-coupled plasma deep reactive ion etching (ICP DRIE) process (Fig. 2(b)). Silicon oxide film was formed on the



Fig. 2. The flow chart of the packaging process.



Fig. 3. A top view of the fabricated via hole and a cross-section scanning electron microscope (SEM) image of a $120 \,\mu m$ diameter via through a $520 \,\mu m$ thick silicon wafer formed using ICPRIE. The wafer with holes was bonded with a seed wafer using a conductive paste.

surface and on the sidewalls of the holes by means of a furnace (wet oxidation) (Fig. 2(c)) at $1000 \,^\circ$ C. The silicon wafer was attached to another substrate coated with a gold seed layer by means of a thick conductive ink (Fig. 2(d)). The holes were, then, filled with copper by electroplating (Fig. 2(e)). The seed substrate was, then, separated from the packaging wafer by removing the conductive ink. In addition, thick PR molds were fabricated to contact bumps. Gold was plated in the PR molds. A non-conductive B-stage epoxy was used to form a sealing line at the external dicing area (Fig. 2(f)). The seal ring and the pads of the device were bonded by low temperature epoxy bonding (Fig. 2(g)).

2.1. Through-hole etching

A number of techniques are available for forming the through holes in silicon wafers, including ultrasonic drilling, mechanical drilling, laser (hologram, excimer), and ICPRIE (inductively coupled plasma reactive ion etching). In this research, we fabricated holes of 120 µm diameter using ICPRIE, which yielded a good aspect ratio and reduced the feature size. The RIE conditions were as follows: the gas ratio was $SF_6:O_2 = 10:1$; the applied RF power was 800 W; the working vacuum had a pressure of 2.93 Pa; the etching rate was 2.5 µm/min; and the depth of the hole was approximately 520 µm. Fig. 3 shows a SEM photograph of the fabricated via hole. The fabricated via hole was etched for 1 min in a hydrofluoric acid (HF) solution to remove the etch passivation polymer because the adhesion of the metal used for the electric connection would otherwise be reduced. A furnace treatment, as described above, completed the preparation of the wafer by oxidizing all of the surfaces.

2.2. Electroplating

Filling methods such as printing and vacuum suction of a conductive paste have been usually used in LTCC (low temperature co-fired ceramic) or MCMs (multi-chip modules). But, when the conductive paste is cured, this method often has problems such as shrinkage or micro-cracking of the paste because of thermal stress. Therefore, in this research simple, low temperature process of electroplating was used for filling the holes. We chose copper for a filling material because of its low resistance. First, the seed wafer was spin coated with conductive

paste. Conductive paste can be made by crushing an adhesive stick into a powder and mixing it into a solution of 4 parts nmethylpyrrolidon (NMP) to 1 part crystalbondTM 509 by weight. To this solution we added 67% by weight of silver powder with a 5 µm particle size. The suspension was coated onto a seed wafer. The solvent was allowed to evaporate for a minimum of 5 min. Unless care is taken to eliminate particles inside the micro-vias, voids can occur within the plated metal. This problem can be reduced by pretreating the wafer with a combination of air agitation and ultrasonic vibration. This is effective in removing particles. After the pre-treatment, the copper was conformally electroplated using a pulse-reverse technique with a forward pulse of 10 mA/cm^2 for 1 ms and a reverse pulse of 2 mA/cm^2 for 3 ms. We, then, used chemical-mechanical polishing (CMP) to remove the excess electroplated copper outside the surfaces of silicon. Fig. 4 shows photographs of a hole filled with copper. Via holes were filled with copper without any voids, micro cracks, or residual stress. To connect the pads of the device to the corresponding tracks metallised on the capping glass, we formed wafer level bumps by electroplating. To obtain the fine grain, good adhesion, and low resistance of the bump, we applied a 5 mA periodic reverse pulse current. Fig. 5 shows the fabricated wafer-level bumps using a gold electroplating method. The height and width of formed bumps were $15 \,\mu m$ and $110 \,\mu m$, respectively. The deviation of the bump height, which was an important factor affecting the quality of the bonding was within $\pm 2\,\mu m$ at the wafer level. This showed very good uniformity. After bonding, the total resistances of contact and feed-through were $0.5 \pm 0.3 \Omega$.



Fig. 4. A SEM image of the cross-section of a Cu-filled via.

Table 1		
Comparison of different adhe	sive bonding techniques	
	Polvimide	S

	Polyimide	SU-8	Parylene	BCB	Epoxy
Bonding temperature (°C)	160	90	230	250	150
Bonding time (min)	60		30	~ 16	30
Bonding strength (MPa)	8.2	20.6	>3.6	>30	>14
Void sources	Release of solvents	Bonding agents	Dirt particles	Release of solvents	Release of solvents
References	[8]	[12]	[13]	[14]	This work



Fig. 5. Photographs of the wafer-level bumps.

2.3. B-stage epoxy patterning and bonding

When the devices and the capping substrate were bonded to protect the devices from contamination or moisture, we attempted low temperature wafer-level packaging by using a non-conductive B-stage epoxy as an intermediate material. The selected intermediate layer material must have patternable characteristics, low glass transition temperature (T_g), and high viscosity. The bonding should have excellent adhesion and produce low residual stress. Polymers used for low-temperature bonding include polyimide (from DuPont) [8], SU-8 (from Microchem Co) [12], Parylene (from DuPont) [13], and BCB (from Dow Chemical) [14], as listed in Table 1. They are usually coated onto the bonding surfaces as a viscous liquid, and then cured at a moderate temperature to create a solid bonding layer.

In this work, we patterned the B-stage epoxy on the 4-in. capping glass by screen-printing. The line width of the mask



Fig. 6. Photographs of the screen printed B-stage epoxy (a) and general epoxy (b).

was 500 μ m. Fig. 6 shows the screen-printed B-stage epoxy and normal epoxy. The B-stage epoxy produced a better pattern definition. B-stage epoxy required a two-step cure process to first remove the solvent and then cure the resin. If the solvent was not sufficiently removed from the adhesive prior to resin cross-linking, voiding in the adhesive bonding line may result. After printing epoxy with a silk-mask, it was soft-baked on a hot plate at 90 °C for 5 min to remove the solvent. The epoxy patterned capping glass and the device substrate with electroplated vias were then aligned using an optical vision system. The aligned wafer pair was placed in a bonder (TPS-1000A, BNP Science, Korea) for heating in a N₂ atmosphere. The bonding conditions and bonding results for the B-stage epoxy are shown in Fig. 7. The bonding temperature ranged from 90 to 170 °C and the bonding time ranged from 30 to 60 min. For bonding with epoxy as the intermediate layer, contact pressure was applied only to the bonding chip, which was calculated to be 3 kPa.

3. Results and discussion

The bonding quality depended critically on whether the interface was void-free or not. We performed the initial bonding process in a vacuum oven to ensure removal of any trapped bubbles between the bonded surfaces. The amount of pressure applied during the bonding process was critical to the bonding strength. The bonding condition for this sample was $150 \,^{\circ}$ C and 30 min. The thickness and width of the bonding line were 30 and 500 μ m, respectively. Fig. 8 shows the cross-sectional SEM micrograph of a bonded pair. The actual line width was 600 μ m. That is, the line width was increased by 100 μ m after bonding. This result was acceptable for application of the bonded pair to dicing.

Hermeticity testing is related to reliability characterization. Indeed, the degree of hermeticity plays a predominant role in the long-term drift characteristics of a MEMS device. The sample cavity volume was 0.0924 mm^3 (2.8 mm long, 1.1 mm wide, and 30 μ m high). The surrounding B-stage epoxy sealing ring



Fig. 7. The bonding strength at different curing conditions.



Fig. 8. A cross-sectional SEM micrograph of a bonded pair. The section is taken across the sealing line.

was 30 µm high and 500 µm wide. Test samples were placed in an air pressure chamber which was connected to the He leak detector (ALCATEL Inc., DGC 1001). The He leak rate was measured. MIL-STD-883 [15] specifies a reject limit of 5×10^{-8} atm cm³ s⁻¹ for volumes smaller than 0.4×10^{-3} cm³. The measured leak rates of the three samples were in the range of 10^{-6} to 10^{-7} atm cm³ s⁻¹ from the He leak test. The sample did not meet the requirements of the test standard. This was an expected result due to the high permeability of the polymers. A sealing method using the B-stage epoxy rim may be useful for devices intended for short-term use, or those less sensitive to hermeticity, such as microfluidics, sensors or static devices, since B-stage epoxy does not guarantee perfect hermeticity with respect to moisture ingress. We expect that the proposed method can be useful as a packaging method for applications in dry environments.

The bonding strength of the bonded pair for various curing times and bonding temperatures was measured by pull testing. The tensile strength measurements were carried out with 10 samples. When the bonding temperature for epoxy was between 150



Fig. 9. An optical photograph of a B-stage epoxy sealed packaging of MEMS device using a silicon cap on a glass substrate.

and 170 $^{\circ}$ C, the bonding strength reached its maximum. In this case, epoxy curing time did not make any difference in the bonding strength. Examining the epoxy-bonded pair, we found that the entire bonding interface was void-free as shown in Fig. 9. Thus, the B-stage epoxy, as the intermediate bonding material, offered the very strong bonding strength of the packaging process. Generally, epoxies are very weak in humidity or water. We dipped the bonded pairs into water to measure the effect of the moisture. After 40 h in water, the tensile strength of the bonded pairs started to decrease. But up to 40 h, the tensile strength was independent of the dipping time.

4. Conclusions

We demonstrated a wafer level packaging method that offered low temperature bonding and low losses. By realizations of the vertical feed-through and the wafer level process, excellent performance was achieved as evidenced by the higher density, low cost, low losses with small parasitic inductance, and better capacitance and signal path lengths. The electroplating condition was carefully tested and applied to obtain a flat surface in the via filling and a bump formation process for uniform contact in the bonding step. The B-stage epoxy, as an adhesive bonding material, was patterned on the 4 in. capping glass by screen-printing. The optimal bonding temperature and curing time were $150 \,^{\circ}C$ and 30 min, respectively. The B-stage epoxy showed good water resistance and tensile strength. We expect that the proposed low temperature adhesive bonding with B-stage epoxy can be applied to wafer-level packaging of many MEMS devices.

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