Efficient suppression of charge trapping in ZnO-based transparent thin film transistors with novel $Al_2O_3/HfO_2/Al_2O_3$ structure

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Charge trapping is dramatically suppressed in ZnO transparent thin film transistors (TFTs) employing a multilayered gate insulator with HfO_2 layer sandwiched by Al_2O_3 layers. In spite of its high dielectric constant, HfO_2 has critical drawbacks including huge charge trap density in interfaces. We suggest and demonstrate an elegant solution to minimize the charge trapping introducing Al_2O_3 buffer layers. The operation of $Al_2O_3/HfO_2/Al_2O_3$ multilayered gate-insulator structure in the ZnO transparent TFT is evaluated to ensure the voltage difference in the hysteresis loop as low as 0.2 V, and the immunization to the threshold voltage shift induced by repeated sweeps of gate voltage. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2924769]

Quite recently, oxide semiconductors have emerged as promising post-Si materials for next generation thin film transistors (TFTs).[1–4] Especially, ZnO has attracted wide attention with its notable advantages over the other semiconductors including a wide direct band gap of 3.37 eV, high transparency in the visible range (400–700 nm), and high mobility. Additionally, it also has good thermal stability, large exciton binding energy (60 meV), and high optical gain (300 cm^{-1}) at room temperature promising a very strong violet luminescence of bound excitonic emissions. So far, diversified ZnO-based materials, such as ZnO, Ga-doped ZnO (GZO), In_2O_3–ZnO, zinc tin oxide, In_2O_3–Ga_2O_3–ZnO, and In_2O_3, have been extensively researched targeting for transparent TFTs, one of the state-of-the-art technologies in which the advantages of ZnO can be maximized.[3–12] Unfortunately, most popular transparent TFT structures employing SiO_2 as dielectric material that has low dielectric constant (k) resulting in low channel modulation effect. Therefore SiO_2-based structures should require high driving voltage to achieve the same operating efficiency compared with the other structures incorporating high-k dielectrics. Moreover, in order to have the equivalent insulation efficiency, SiO_2 dielectric layer should be thicker than high-k materials. To solve the problems originated from using the low-k materials, we explore high-k dielectric materials to find that HfO_2 is one of the most promising materials due to its remarkable properties highlighting (i) high dielectric constant (~25), (ii) relatively low leakage current, (iii) low synthesis temperature, (iv) large band gap (5.68 eV) sufficient to yield a positive band offset with respect to ZnO, and (v) high transparency over a wide spectral range extending from the ultraviolet to the midinfrared.[3,13] However, it has a critical drawback, high charge trap density mainly being concentrated into the interfaces between gate electrode and gate insulator, as well as gate insulator and channel layer.[14,15]

In this paper, we dramatically suppress the trapping and the leakage current with very thin Al_2O_3 buffer layers that act as good barriers with the tolerable expense of the dielectric property.[16] The buffer layers are added to form a novel $Al_2O_3/HfO_2/Al_2O_3$ (AHA) dielectric structure to reduce the deleterious effects on both top and bottom interfaces. Most importantly, hysteresis that deteriorates device performances is minimized preventing charge trap at the interfaces between active layer and dielectrics. The operation of the HfO_2–Al_2O_3 alternating structure is evaluated to measure that the voltage difference in the hysteresis curve is ~0.2 V. The resultant device is immunized to the threshold voltage shift induced by the repeated sweeps of gate voltage.

Glass substrates are cleaned in an ultrasonic bath with acetone, methanol, and de-ionized water, respectively. ZnO thin films of 50 nm are deposited on glass substrate at 500 °C by rf-magnetron sputtering method. The power and partial pressure of mixed Ar and O_2 are maintained to 150 W and 10 mTorr, respectively. In general, since the conductivity of ZnO channel is too high, we try to decrease the thickness of ZnO thin film in order to reduce the total number of defects, such as zinc interstitials and oxygen vacancies. Active layer is patterned by conventional photolithography process. Drain-source and gate electrodes of transparent GZO are deposited at room temperature using pulsed laser deposition. 5 wt % GZO is used as the target for electrodes. The target and the substrate are simultaneously rotated at 4 rpm to improve the uniform laser ablation and deposition of the ablated particles onto the substrate. The basal vacuum in the chamber is lower than 1×10^{-5} Torr, and energy density, target-substrate distance, and oxygen partial pressure are 1.6 J/cm^2, 4 cm, and 5 mTorr, respectively. Thickness of GZO films is maintained to about 130 nm to keep high transparency at the center wave length of 550 nm for visible region. Note that the film thickness approaching $\lambda/4$ has high transparency in visible region. Also, sheet resistance of deposited GZO film is measured to have the value lower than 5 Ω/sq. HfO_2 thin film used as the main gate insulator is deposited at room temperature by a rf-magnetron sputtering method. Here, the thickness of HfO_2 thin film is adjusted to about 200 nm since the gate insulators of more than 200 nm thickness are normally needed to ensure pinhole-free

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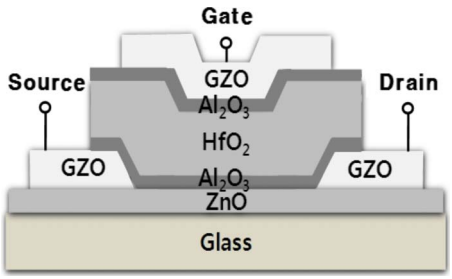
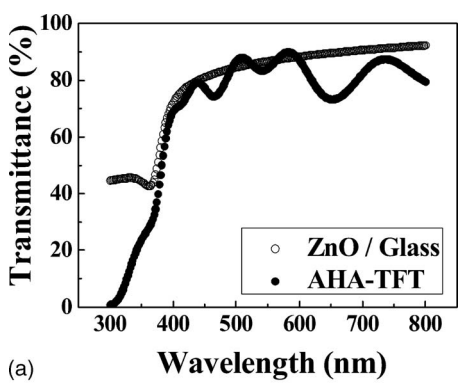


FIG. 1. (Color online) Schematics of ZnO-TFT with the novel gate-insulator structure of AHA [ZnO (50 nm), Al_2O_3 (10 nm), HfO_2 (200 nm), GZO (130 nm)].

coverage.[17] Al_2O_3 thin films of 10 nm which are used as barrier layers in order to preventing interface charge trap are deposited at room-temperature using rf-magnetron sputtering. We design and construct the resultant gate-insulator structure of Al_2O_3 (10 nm)/HfO_2 (200 nm)/Al_2O_3 (10 nm). Gate-insulator layers, drain-source, and gate electrodes are patterned by conventional lift-off process in order to suppress the damage from etching process. The channel width and length are 500 and 50 μm, respectively.

Figure 1 shows the TFT structures with the gate-insulator structure of AHA. The high-k 200-nm-thick HfO_2 layer is used as the main gate insulator sandwiched by the 10-nm-thick Al_2O_3 layers that are used as barriers to suppress the charge trap in the interfaces formed between gate electrode and gate insulator, and between gate insulator and active layer. As a result, HfO_2 layers with high charge trap density could provide a possible leakage path, but it is expected that the leakage current can be reduced employing Al_2O_3 barrier layers. The optical transmission measurement of the device is performed using a UV-Visible spectrometer (Perkin Elmer, 300–800 nm). Figure 2(a) shows the transmittances of ZnO thin film on glass substrate and AHA-TFT structure of GZO/Al_2O_3/HfO_2/Al_2O_3/GZO/ZnO on glass



(b)

FIG. 2. (Color online) (a) The optical transmission spectra of ZnO/Glass, and AHA-TFT of GZO/Al_2O_3/HfO_2/Al_2O_3/GZO/ZnO/glass structure. Average transmittance of the device is over 80%. (b) Comparison of the transparency between the pure glass (left) and the devices on the glass substrate (right).

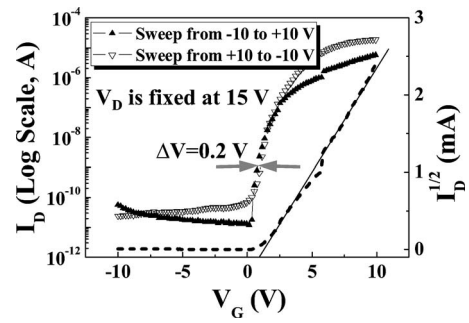


FIG. 3. Transfer characteristic of ZnO-TFT with gate-insulator of AHA structure. Up triangles show positive sweep from −10 to +10 V and down triangles show negative sweep +10 to −10 V at V_G=15 V, respectively. Dashed line shows square root of drain current.

substrate. The average transmittance of the ZnO and the AHA-TFT on the glass substrates are about 85% and 80%, respectively, in visible region. The electrical properties are measured by four-point probe method. Figure 2(b) shows the transparent final devices depicting that the transparency of the devices on the right is comparable to that of the pure glass located on the left. The current-voltage (I-V) characteristics are obtained with a semiconductor parameter analyzer (HP4145B, Agilent). Figure 3 shows the transfer characteristics of ZnO-TFT with the gate insulator of the AHA structure. The on-to-off current ratio was measured to be about 5×10^5 for the operation in the saturation region. The channel mobility and threshold voltage are calculated by linearly fitting the square root of I_D versus V_G curve of the transistor operating in the saturation region. The following is the expression for the operation of a field effect transistor in the saturation region:[18]

$$I_D = \left(\frac{C_i \mu_{\text{sat}} W}{2L}\right)(V_G - V_{\text{th}})^2 \quad \text{for} \quad V_D > V_G - V_{\text{th}}, \qquad (1)$$

where W is the channel width, L is the channel length, C_i is the capacitance per unit area of the gate insulator, I_D is the drain-to-source current, V_G is the gate voltage, and V_{th} is the threshold voltage of TFT. Drain current is function of gate voltage. The estimated field effect mobility (μ_{sat}) in the saturation region is ~12 cm^2/V s, and V_{th} is estimated to about 1.0 V. We can observe that hysteresis is suppressed in this TFT structure, voltage difference is measured to be only about ~0.2 V at 10^{-9} A. The current level of 10^{-9} A is defined to be the "turn on" current level as is 100 times higher than that of the "off current" that is the current with the zero-gate bias as can be found in the curve (see Fig. 3). Also, we check the threshold voltage shift by measuring the voltage 50 times to find that there is negligible shift. Figure 4 shows the threshold voltage changes according to the repeated measurement for 50 times to find that the threshold voltage shifts from 0.94 to 1.54 V, and the mean value of the threshold voltages is 1.24 V. In case the charge trap in the interfaces exists, transfer characteristic curve should be shifted, however, the curve shift observed is negligible while repeating the measurement for 50 times ensuring the successful operation of the double buffered AHA-TFT structure. This result indicates that the Al_2O_3 layers show good performance as barriers for the suppression of the charge trap at the interfaces.[19,20] The device shows weak hysteresis characteristics even though charge trap is sufficiently suppressed by Al_2O_3 barrier layer. This is mainly due to the induced charge

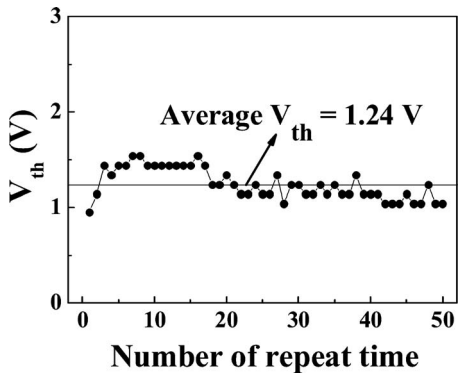


FIG. 4. Threshold voltage shift with 50 times checks. Threshold voltage is varied from 0.94 to 1.54 V, and average threshold voltage is measured to 1.24 V.

trap at the interface between Al_2O_3 layers and other layers, but this effect is relatively small as reported before.[21,22]

In summary, we demonstrate the suppression of the interface charge trap by introducing the AHA gate-insulator structure to ZnO-based transparent TFT. The gate insulator comprises the sandwiched HfO_2 layer with the Al_2O_3 buffer layers on top and bottom. In result, hysteresis characteristics can be dramatically suppressed by using the Al_2O_3 layers mainly due to the prevention of charge trapping at the interface. With the novel AHA structure, very stable operation of the device performance is observed. The saturation mobility (μ_{sat}), on-to-off ratio, threshold voltage, and subthreshold swing are $\sim 12\ cm^2/V\ s$, $\sim 5\times 10^5$, 1.24 V, and 0.52 V/decade, respectively. The average optical transmittance in the visible region is observed over 80%. It is expected that this elegant AHA-TFT structure with very low hysteresis characteristics will be a possible candidate for stable backplane TFT to replace amorphous-Si for future display applications.

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