A thermocompressive bonding method using a pure sputtered Au layer and its wafer scale package application

Jongseok Kim
Display and Nanosystem Laboratory, College of Engineering, Korea University, Anam-dong, Seong buk-gu, Seoul 136-701, Republic of Korea and Samsung Advanced Institute of Technology, Nongseo-Dong, Giheung-Gu, Youngin-Si 449-712, Korea

Sangwook Kwon, Youngteak Hong, and Insang Song
Samsung Advanced Institute of Technology, Nongseo-Dong, Giheung-Gu, Youngin-Si 449-712, Korea

Byeongkwon Ju[a)]
Display and Nanosystem Laboratory, College of Engineering, Korea University, Anam-dong, Seong buk-gu, Seoul 136-701, Korea

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The authors have developed a thermocompressive bonding method using a sputtered Au layer and applied it to the coplanar waveguide (CPW) package. The bonding temperature is 350 °C, the bonding pressure is 63 MPa, and the duration time is limited to 30 min. The bonding strength is evaluated using the Scotch tape and tweezers detaching method and the hermeticity is evaluated using helium leak detection work station. The measured hermeticity is 1.0×10^{-9} Pa m^3/s. To measure the electrical properties, the CPW line is packaged and the rf characteristics and dc resistance are measured. The insertion loss of the packaged CPW line is −0.074 dB at 2 GHz and the dc resistance is from 0.019 to 0.046 Ω. This result shows that their Au compressive bonding method is very useful and good for microdevice wafer level packaging applications.
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I. INTRODUCTION

Many institutes and companies have been developing microelectromechanical system devices such as accelerometers for air bags, rf devices, pressure sensors, chemical sensors, etc.[1–4] Most of these devices consist of microsized structures or membranes that are very easy to break or damage, so they need to be hermetically sealed against moisture, dirt, air, and various kinds of contamination sources or mechanical and radiation loads. Sometimes they should be packaged in a vacuum or at a specific vacuum level in order to keep the internal moving parts operating in a stable manner. In order to seal these device wafers with a cap wafer, wafer bonding technology must be used. Silicon direct bonding (SDB), anodic bonding, and intermediate layer bonding are representative silicon bonding methods.[5–11] SDB is very critical to the bonding surface, so it needs a very clean environment, a high temperature, or plasma activation for low temperature bonding.[12] Anodic bonding needs a high electric field and it is limited to the glass wafer as a cap wafer. Intermediate layer bonding needs a bonding layer such as Au–Sn, frit glass, Au, solder, or indium. Heat and compression are applied to the surfaces of the two wafers to weld the interface of the bonding layer.[13]

Au bonding is a very reliable and robust bonding method.[14,15] Compared to Au–Sn or solder layer, the native oxide on the metal layer is not generated. This layer is an obstacle when bonding the face layer and it reduces the bonding strength. Only pure thin Au metal is used as a bonding layer, and it produces a very stable and reproducible bond compared to the eutectic bonding method or the thick Au electroplating layer. During the bonding process, little outgassing occurs. In this experiment, we investigate the thermocompressive bonding of a sputtered pure thin Au layer and present a microdevice packaging method. The coplanar waveguide (CPW) line is packaged and the rf and dc performances are evaluated.

II. EXPERIMENT

We used high resistivity silicon (HRS) for bonding the test wafer. Its resistivity is over 10 000 Ω cm and it is a 4 in., *n*-type wafer. This high resistivity silicon wafer reduces the substrate loss of rf signals. Figure 1 shows the fabrication process flow of the test wafer. After an initial cleaning process, a 1 μm thick thermal oxide was grown by wet oxidation to make the wrinkle shape pattern. A GXR 601 photoresist was coated on the oxide layer by a spin coater and patterned. The oxide was etched by Unaxis induced coupled plasma reactive ion etcher (ICP-RIE) equipment and an Asher was used to remove the GXR 601. The width of the protruded wrinkle pattern was 5 μm and the width of the groove was 6 μm.

The bonding layer of Cr/Au (50/1000 nm) was deposited using sputtering equipment. The GXR 601 photoresist was coated on the sputtered Au layer and patterned. The Cr/Au layer was etched by using the wet etching method. After the etching process, we etched the whole exposed silicon layer by ICP-RIE to form the cavity of the cap wafer. At this time, the sealing line and contact pad were formed simultaneously.

a)Electronic mail: bkju@korea.ac.kr

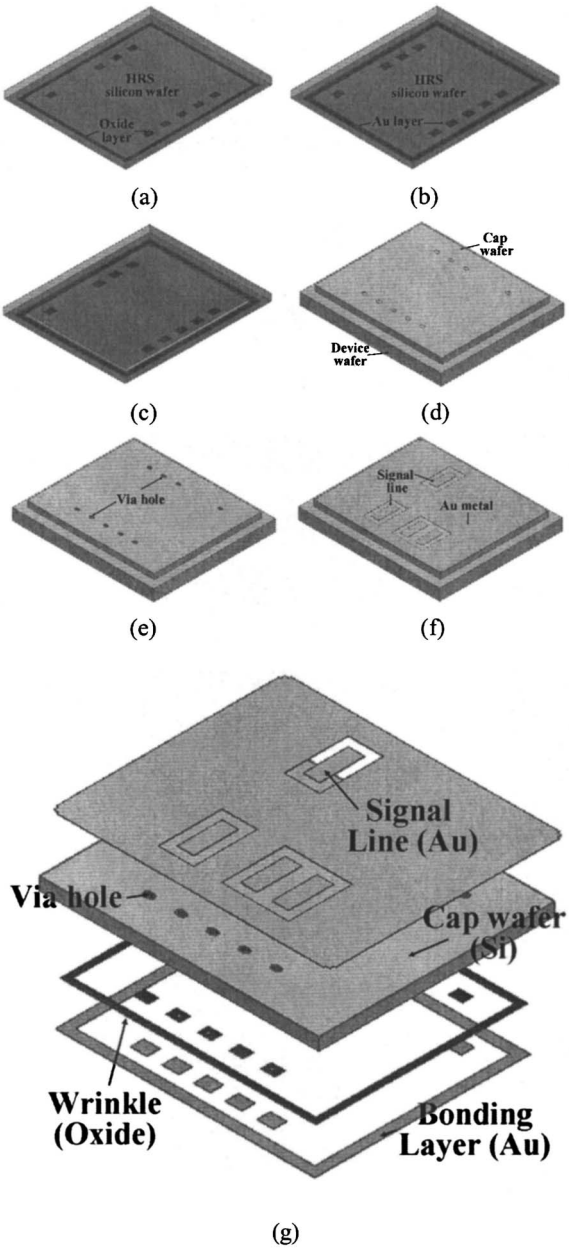


FIG. 1. Fabrication process flow for bonding the test cap wafer: (a) oxide layer deposition and patterning, (b) Au layer deposition and patterning, (c) cavity formation by silicon etching, (d) bonding with the device wafer and polishing, (e) via hole patterning and etching, (f) metal layer sputtering and patterning, and (g) each fabricated layer is spreaded perpendicularly.

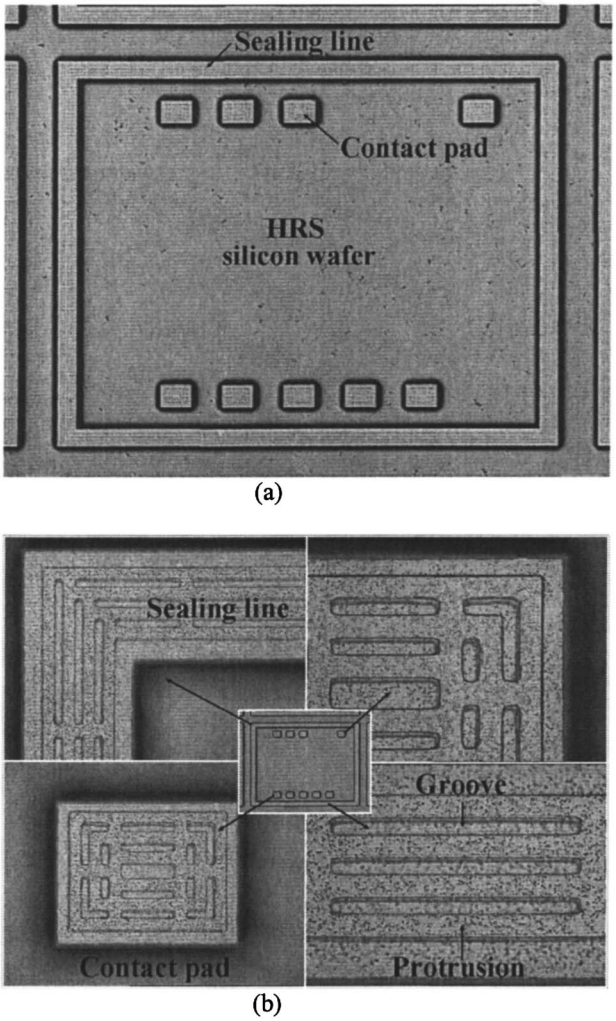
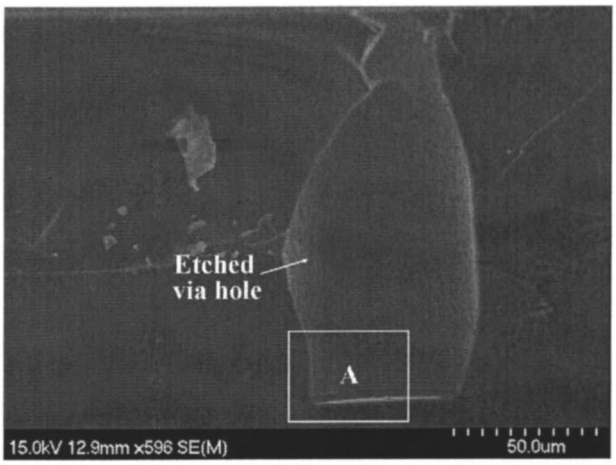
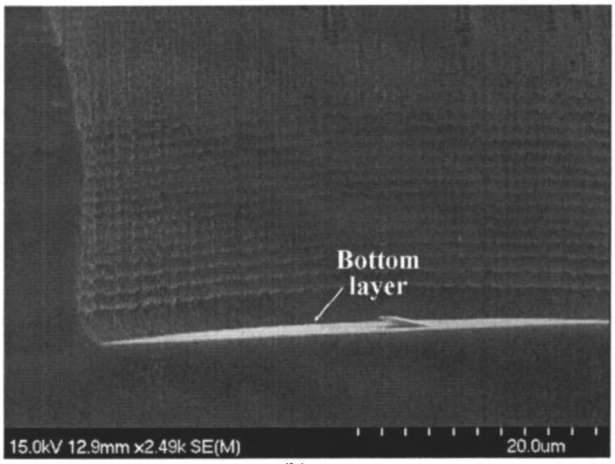


FIG. 2. Microscope image of the fabricated cap wafer: (a) microscope image of the fabricated cap wafer and (b) magnified image of the contact pad and the sealing line.

The etched depth of the cavity was 50 μm and its size was 1915×1560 μm^2. The sealing line width was 50 μm and the contact pad size was 110×83 μm^2. The patterned GXR 601 was removed by the Asher and wet cleaning was performed to remove the extra residues or organic contaminants before the bonding process. A $H_2SO_4:H_2O_2=1:1$ mixed solution was used to clean the wafer, and its dipping time was 1 min. On the device wafer, the patterned Cr/Au layer for bonding had to be placed, but the wrinkle shape was not needed. The recommended thickness of this layer is over 50/100 mm and the linewidth is 120 μm. This wide width of bottom layer minimized the misalignment failures during the bonding process because the 50 μm wide bonding pad of the cap wafer only needed to bond with the Au layer of the bottom bonding pad. The fabricated cap wafer is shown in Fig. 2. The device wafer and cap wafer were aligned by using the EV-620 bond aligner and they were placed into the bonder. An initial pressure was applied to prevent any tilting of the alignment while pumping or heating. The tested temperature range of the bonding process was 320–360 °C, the pressure range was 13–63 MPa, and the hold time was set to 30 min. After the bonding process, grinding and polishing were performed over the cap wafer until the cap wafer was 150 μm thick. On the grinding side, a via hole for the signal interconnections was patterned and etched by the ICP-RIE. A low frequency recipe was used to minimize the notching effect.[16,17] The shape of the via hole was an elliptical design because the sputtered metal is easy to deposit on the bottom and sidewalls compared to the small size of a circle hole. The dimensions of this elliptical hole are 80 and 50 μm. Figure 3 shows a scanning electron microscopy (SEM) image of the



(a)



(b)

FIG. 3. SEM image of the via hole of the low notching test wafer: (a) cross sectional view of the via hole and (b) magnified "A" area.

via hole and the notching of the test wafer. The etched sidewall is vertical and notching is not generated during the dry etch process.

A Cr/Au 50/2000 nm thick layer of metal was sputtered on the cap wafer to form the interconnection metal line instead of metal filling method.[18–21] A PR spray coater was used to pattern the metal layer. This coater can overcome the coating of the via hole edge line, which was not coated when we used a normal spin coater and it could easily break down during the wet etching process. The Cr/Au was patterned by using a wet etchant and the PR was removed by using the wet solution. The bonding strength of the packaged CPW line was measured roughly by detaching the cap wafer using Scotch tape and tweezers. Scotch tape test is widely used for evaluating the adhesion of deposited thin film.[22] The dc resistance and the rf characteristics were measured to evaluate the interconnection performance. The bonded and detached interfaces were observed using a SEM image. The hermeticity of the bonding test wafer was also measured using the Alcatel DGC 1001 helium leak detection work station.

TABLE I. The bonding conditions of the tested wafer. (Bonding duration time: 30 min.)

Test No.	Temp. (°C)	Prssure (MPa)	Results
1	320	27	Partially
2	320	63	Weakly
3	360	13	Partially
4	350	27	Weakly
5	350	63	Strong

III. RESULTS AND DISCUSSIONS

Table I shows the bonding conditions of the tested wafer and the test results. The temperature range of the bonding process was 320–360 °C and the pressure range was 13–63 MPa. The duration was limited to 30 min because excessive exposure to the high temperature sometimes degrades the performance of the device. The bonding quality was evaluated by detaching the cap wafer. Partially bonding means that the bonded silicon caps are detached when using the Scotch tape and tweezers. The bonded Au layer was cleanly separated without leaving any of the layer on the opposite side, so only the marking remained. Weak bonding means that some of the bonded silicon cap is detached by the Scotch tape. But, some of the bonded silicon cap remains. The bonding strength was stronger than weak bonding, but most of the Au layer was separated without transferring to the opposite side. Figure 4 show the detached silicon cap wafer of the sample in test number 5. Strong bonding means that the silicon caps are not detached by the Scotch tape. When we detached the silicon cap using tweezers, the silicon cap was broken or Cr/Au bonding pad was transferred to the opposite side like Fig. 4(a). The color of transfered Cr layer was metallic white. So, Au layer was not diffused into Cr and bottom silicon. In some cases, the Au layer with the bottom silicon was broken and transferred to the opposite side. In order to evaluate the metal interconnection, we bonded the cap wafer with the CPW line and patterned a dummy wafer.[23,24] The CPW line was fabricated on the HRS wafer and the thickness of the Au metal line was 1 μm. The resistance of the packaged samples was also measured using the four point method. The measured points were the signal line to signal line on the cap wafer. Table II shows the measured resistance of the tested samples. All of the measured patterns showed a very low resistance. Figure 5 shows the rf characteristics of the packaged CPW dummy pattern. Test no. 5 condition is used to bond the CPW line pattern with package cap wafer. An HP 8753D network analyzer was used to analyze the rf characteristics of the package sample. The insertion loss of the CPW line was −0.043 dB at 2.0 GHz and the insertion loss of the packaged CPW line was −0.074 dB at 2 GHz, so the package loss of our design was −0.03 dB. The hermeticity of the bonding test wafer was also measured using the Alcatel DGC 1001 helium leak detection work station. The measured leak rate of the bonding test sample was

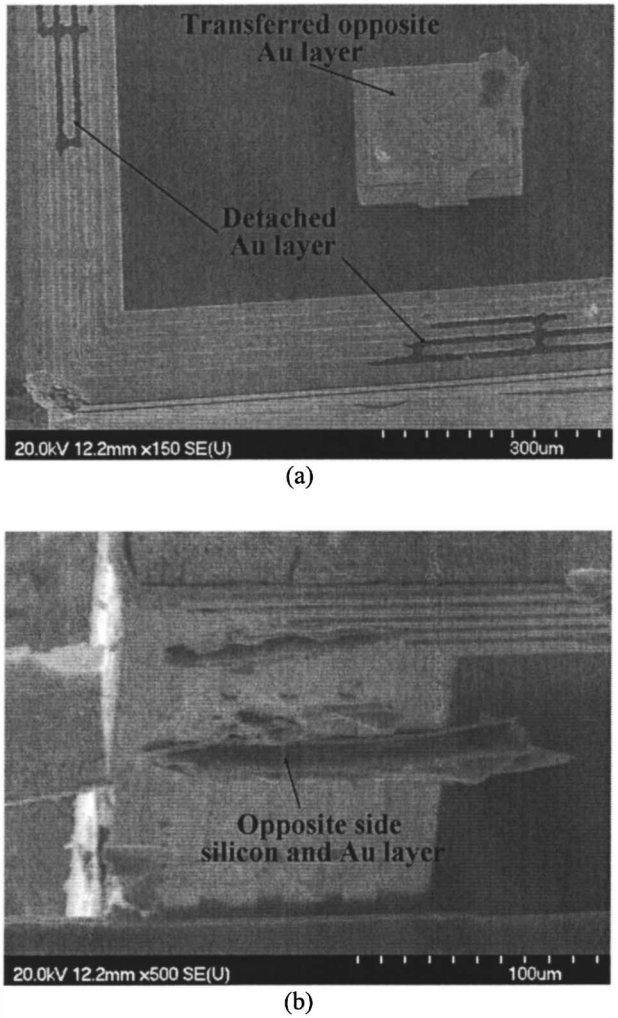


FIG. 4. SEM image of the detached cap wafer: (a) the bottom Au layer was transferred to the cap wafer and (b) the bottom silicon layer was transferred to the cap wafer.

1.0×10^{-9} Pa m^3/s. According to MIL-STD-883, the hermeticity limitation for a volume smaller than 0.40 cm^3 is 5.07×10^{-9} Pa m^3/s.[25]

IV. CONCLUSION

A thermocompressive bonding method using a sputtered Au layer was developed, and we applied it to the CPW line wafer scale package. The bonding temperature was 350 °C and the bonding pressure was 63 MPa for 30 min. The bonding strength was measured using Scotch tape and tweezers.

TABLE II. Measured resistance of the CPW line package (unit: Ohm).

Top	0.019	0.021	0.028
Center	0.024	0.024	0.028
Bottom	0.026	0.024	0.033
Left	0.027	0.026	0.021
Right	0.025	0.024	0.046
Mean		0.026	
St dev.		0.0064	

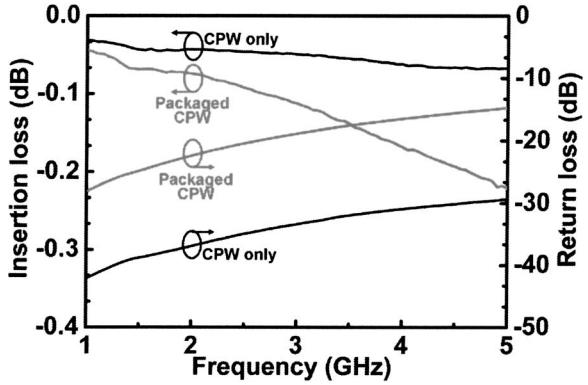


FIG. 5. Measured insertion loss of the packaged CPW line.

When we detached the silicon cap, it broke or the bonded Au layer was transferred to the opposite side. Sometimes the Au layer with a silicon pillar was transferred to the opposite side. The rf characteristics of the package were evaluated using the CPW line package. The insertion loss of the packaged CPW line was −0.074 dB at 2 GHz. Its loss level was very low compared to other packaging methods. These test results showed that our Au compressive bonding performs well, so we expect that this method will be good for improving the yield of microdevices that are packaged at the wafer level.

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