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ABSTRACT

This paper presents design, fabrication and evaluation of a wafer level MEMS (Micro Electro Mechanical System) encapsulation using an Au to Au direct bonding with wrinkle patterned layer. For the effective encapsulation, the optimal bonding condition, the bonding temperature 350 °C, the bonding pressure 58 MPa and the duration time 30 min, was developed and used in this paper. We briefly evaluated the bonding strength of test wafers after the bonding test. For RF (Radio Frequency) device packaging, we effectively interconnected Au CPW (Coplanar Waveguide) lines to feedthroughs and measured the RF characteristics. Measured insertion loss of the packaged CPW line was −0.11 dB at 2 GHz. The glass wafer having patterned Au sealing lines was also bonded and has been dipped in the acetone solution for 24 h to examine the leakage of bonding wafer. After 24 h dipping, any leakage point has not been observed at the sealing line and inside the cavity. These results showed that our Au to Au direct bonding method is very reliable and suitable for RF device packaging.

1. Introduction

Most micro-mechanical devices such as a accelerometer, a gyroscope and a pressure sensor consist of delicate micro-sized moving structures that are very easy to be damaged from moisture, dirt, and air etc. [1–4]. For these certain circumstance to applications, micro devices could be encapsulated under desired pressure and ambient [5]. Among these micro devices, RF micro-mechanical device must package not only hermetic sealing condition, but also low RF signal loss condition. RF signal loss is caused by impedence mismatch, or electrical high resistance of signal line and interconnection line. The packaging cost of small sized devices can reach more than 70% of the total expense. However, fortunately most packages use a die level process and its total cost can be reduced by packaging the device at wafer level. For the effective wafer level encapsulation of device wafer, a wafer bonding technology is indispensable. There are several techniques widely used for bonding technologies [6–8]. Although these bonding technologies can be highly effective and widely used, each one has some limitations. Silicon Direct Bonding (SDB) is very sensitive to the roughness of bonding surface and particles. SDB needs not only a very clean environment, but also a very high bonding temperature or pretreatment. Anodic bonding method that needs a high electric field has limitations in using a glass wafer as a cap or substrate wafer. Thermocompression bonding requires a high-force and a high temperature on a surface. This bonding method has been considered as a standard packaging technique in microelectronics, in both wire and tape automate bonds. Au–Sn, frit glass, Au, solder, or indium are used as bonding materials. Among these bonding materials, Au is the most robust and stable [9]. Au does not generate the native oxide layer which makes a bonding failure or weakens the strength of the metal layer compared with Au–tin or solder layer, and moreover a little outgassing can be occurred during a bonding process. In this study, we develop the RF device package method by using sputtered thin Au film. Sealing line and bonding layer formation method is very simple and easy compared with general Au electroplating method or Au–tin bonding method. We also investigated packaging including CPW line for RF applications and RF characteristics were evaluated. We used only pure thin Au as a bonding layer, and experimentally confirmed that the proposed Au direct bonding is very reliable and reproducible compared with the eutectic or thick Au electroplating layer bonding.

2. Experiment

The whole fabrication process flow of RF micro device package is illustrated in Fig. 1. In order to package the device, we used a High Resistivity Silicon (HRS) wafer as a cap wafer to prevent the signal loss from substrate. Resistivity of this wafer is over 5000 Ω and 4 in. n-type wafer is used. After an initial cleaning process, a GXR 601 photoresister was coated by a spin coater and patterned to form concave–convex pattern at the sealing line. ICP-RIE was used to etch the silicon layer and the depth was 3–4 μm. The width of the convex pattern was 3 μm and that of concave pattern was 2 μm. This layer increase the sealing line width compared with the same bonding area and the bonding pressure is more fully transferred to each bonding layer. After etching process, an Asher

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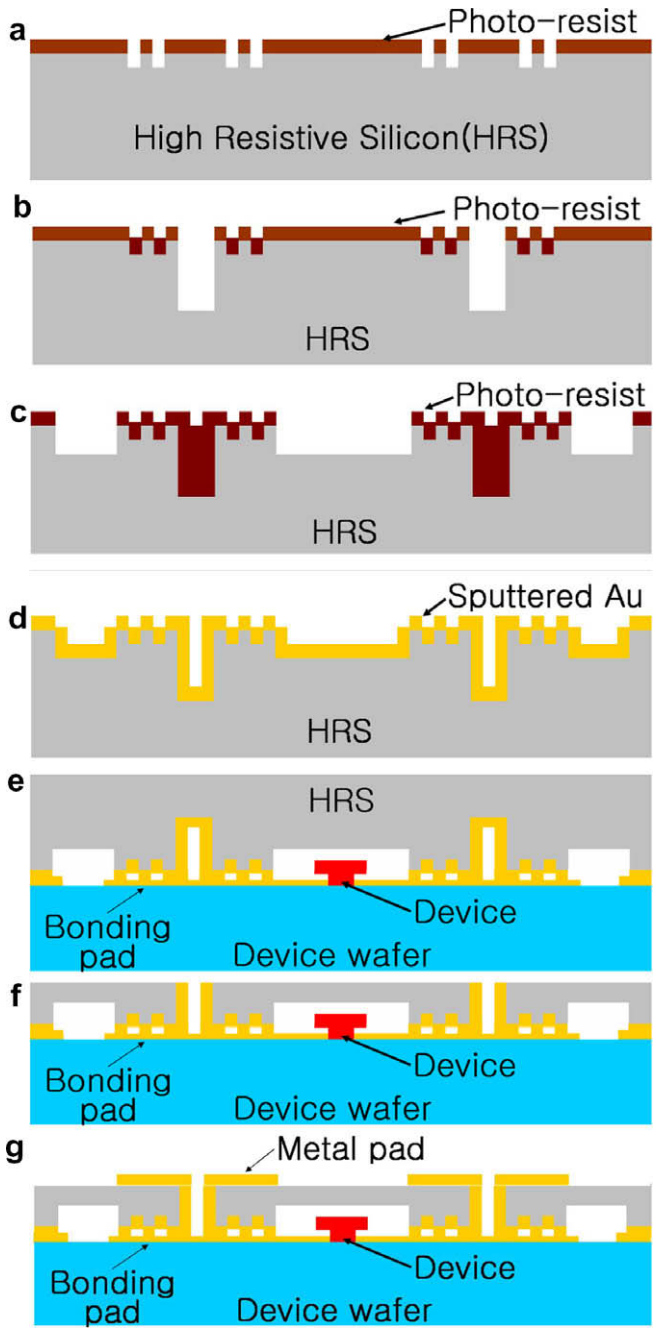

Fig. 1. Fabrication process flow for bonding test cap wafer: (a) convex–concave pattern formation on the silicon wafer, (b) via hole patterning and etching, (c) cavity formation by silicon etching, (d) Au layer deposition and patterning, (e) bonding with device wafer, (f) cap wafer lapping and polishing, and (g) metal pad formation.

was used to remove the GXR 601. To make via holes for signal interconnection lines, GXR 601 was coated, patterned again and 70 μm depth was etched using ICP-RIE (Inductively Coupled Plasma Reactive Ion etcher). Photoresist was also removed using Asher equipment. After ashing process, AZ4330 photoresist was coated and patterned to fabricate the cavity space for a micro device. A spray coater has been used to overcome the 3D structure with a sharp edge of a via hole, which was not uniformly coated when we used a normal spin coater and it could easily etch during cavity etching process. ICP-RIE was used to make a cavity and the etched depth is 5 μm, a cavity size was 900 × 905 μm. During the etching process, the sealing line and the contact pad line were also formed simultaneously. The sealing line width was 20 μm and the contact pad size was 40 × 90 μm. The cavity depth is strongly dependent on both what kinds of devices are packaged and what the maximum height of devices is. After removing of photoresist, Cr/Au (50 nm/1000 nm) for a bonding layer was deposited using a sputtering equipment. On the Au layer, the AZ4330 photoresist was coated using spray coater and patterned. The wet solution was used to etch the Cr/Au layer and the photoresist was removed using asher equipment. The wet cleaning process with H_2SO_4: H_2O_2 = 1:1 mixed solution was added to remove extra residues or organic contaminants before the bonding process and its dipping time was 1 min. Fig. 2 shows the microscope image of the fabricated cap wafer. On the device wafer, the patterned Cr/Au layer for bonding is necessary. The thickness of this layer was 50 nm/1000 nm and the line width was 70 μm. This wider substrate sealing line maximizes the misalignment margin and minimizes the alignment failure during the bonding process because the cap wafer pad only needs to be bonded with the Au layer of the bottom bonding pad. The device wafer was set on the bonding jig and aligned with cap wafer after placed on the EV-620 bonding aligner. Aligned wafers were fixed by using the pin on the bonding jig and moved into the pressure bonder. Before the wafers are placed on the bonding place, it is essential to check the particles on the wafers or on the bonding place because they can lead to wafer breaking or cracking during the bonding process. After closed the bonding chamber, air is pumped out and 0.1 MPa of pressure was applied to the aligned wafer to prevent movement of wafers. Substrate was heated to the setting temperature and wait 10 min. The temperature range of the bonding process was 320–350 °C, the pressure range was 2.4–58 MPa, and the hold time was set to 30 min. After substrate temperature dropped to below 100 °C, the chamber was purged to air and take out the bonded wafer. The silicon cap wafer was grinded and polished until 50 μm thick. Via holes for the interconnections of RF signal line were patterned on the grinded side and etched using ICP-RIE equipment [10,11]. The notching effect was minimized using a low frequency recipe. The shape of the via hole was rectangular and the edge of rectangle was rounded out. The dimension of this hole is 18 × 70 μm. A Cr/Au 50 nm/2000 nm thick layer was sputtered on the cap wafer to

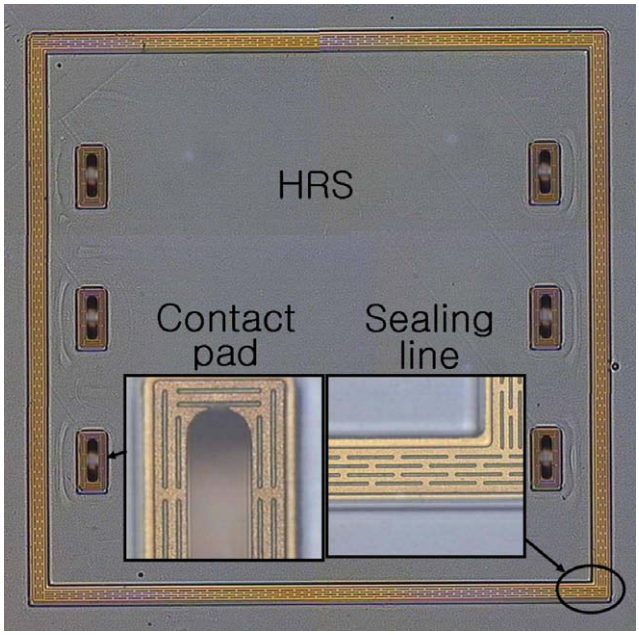

Fig. 2. Microscope image of the fabricated cap wafer.

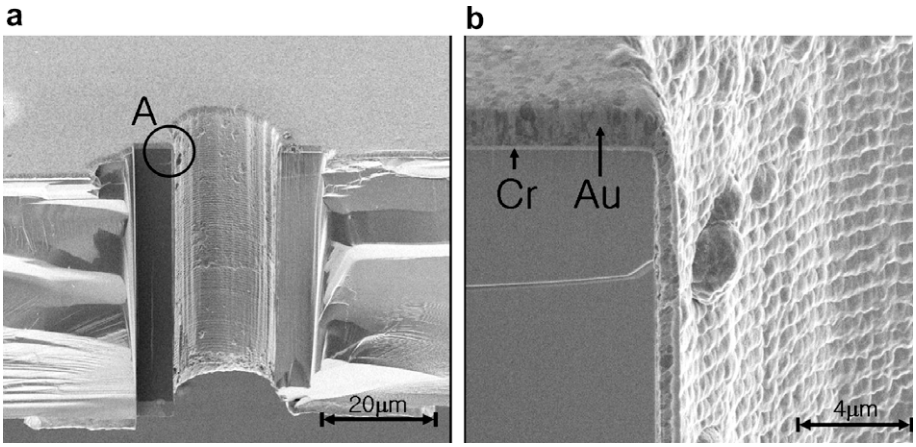

Fig. 3. Cross sectional SEM image of the via hole: (a) via hole metal interconnection, and (b) magnified 'A' area.

form the interconnection metal line and AZ4330 photoresist was used as a etch mask to make a pattern. The patterned Cr/Au layer was etched using a wet etchant and the AZ400T wet solution was used for the removal of the photoresist. The cross sectional SEM image of metal, Fig. 3, shows that interconnections were properly formed through via holes. RF characteristics including interconnection performance are evaluated by packaging the CPW dummy line. After finishing the final packaging process, the bonding strength of the packaged CPW line was measured roughly by scotch tape detaching method, and interfaces of bonded area were observed using SEM after scotch tape detaching [12,13]. 3M Crystal Clear Type tape is used and its adhesion force to steel is 76 g/cm^2. Package test samples were dipped in the acetone and examined whether there is a leakage or not.

3. Results and discussion

Bonding parameters of test wafer and brief test results are shown on the Table 1. The temperature range of the bonding process was 320–350 °C and the pressure range was 2.4–58 MPa. We started this bonding temperature from 320 °C because this temperature is a little higher than normal PCB reflow temperature. The duration time was 30 min because a long time exposure to the high temperature may affect the performance or reliability of the device. The bonding quality was evaluated by detaching the cap wafer. Test numbers 1 and 2 condition wafers easily detached from device wafer in using the scotch tape test. In this test conditions, the bonded Au layer was clearly separated without any remaining on the opposite side of layer and only left a few marks. In consequence of the applied temperature and force not enough to bond of Au to Au atomic layer, that of condition parameter need to be elevated. In the test number 3 condition, most of the bonded silicon cap wafers were detached by the scotch tape. However, some of the bonded silicon cap wafers remained without detaching form the device wafer. The bonding strength was stronger than previous bonding, but majority of the Au layer was separated without being transferred to the opposite side. On the other hands, Fig. 4 shows the detached silicon cap wafer of the sample in the test number 1 and 4 condition. In the test 4 condition, the silicon cap wafers were not detached by the scotch tape. When we detached the silicon cap wafer, it was broken or the bonded Au layer was transferred to the opposite side. Sometimes, the Au layer with the bottom silicon wafer was broken and transferred to the opposite side. Fig. 4c shows the cross sectional SEM image of bonded sealing line. Au on the convex pattern of cap wafer and Au line on the bottom wafer is very well bonded. Cap wafer is interconnected with substrate using via hole and sputtered Au metal is used instead of metal filling method [14]. Interconnection characteristic of the proposed packaging method was evaluated by bonding of cap wafer with CPW line patterned on the dummy wafer. The CPW line was fabricated on the HRS wafer and the deposited Au metal thickness was 1 μm. Fig. 5 shows the RF characteristics of the packaged dummy CPW pattern. An HP 8753D network analyzer was used to measure an insertion loss and a return loss at the broad frequency. The insertion loss of the CPW line was −0.05 dB at 2.0 GHz and the insertion loss of the packaged CPW line was −0.11 dB at 2 GHz, so the package loss of our design was −0.06 dB at 2 GHz. To evaluate the leakage of our sample briefly, the glass wafer with patterned bonding layer was bonded with the cap wafer and dipped in to the acetone solution. After 24 h, we took out the wafer and observed the inside of cavity through the substrate glass. Fig. 6 shows the microscopic image of cavity. The outside of sealing line is filled with acetone solution. But, there was no mark or pattern of acetone solution, observing the inside of the cavity.

Table 1
The bonding conditions of the tested wafer.

Test No.	Temperature (°C)	Pressure (MPa)	Results
1	320	2.4	100% detached
2	350	13	100% detached
3	350	21	About 70% detached
4	350	58	0% detached

Bonding duration time: 30 min.

4. Conclusion

A thermo-compressive bonding method with patterned Au layer was developed, fabricated and tested. Using this method, we packaged the CPW line and evaluated RF characteristics. The bonding temperature was 350 °C and the bonding pressure was 58 MPa for 30 min. The bonding strength was briefly measured using scotch tape detach method. When we detached the silicon cap wafer, it broke or the bonded Au layer was transferred to the opposite side. The RF characteristics of the package were evaluated using the CPW line package. The insertion loss of the packaged CPW line was −0.11 dB at 2 GHz. Glass wafer was also packaged to know the leakage of bonding wafer. After 24 h dipping in acetone solution, we observed the inside of cavity through the glass and there were no marks or no patterns of acetone solution. These results showed that our Au bonding method performs well and is very reliable. Consequently, the proposed wafer level Au to Au di-

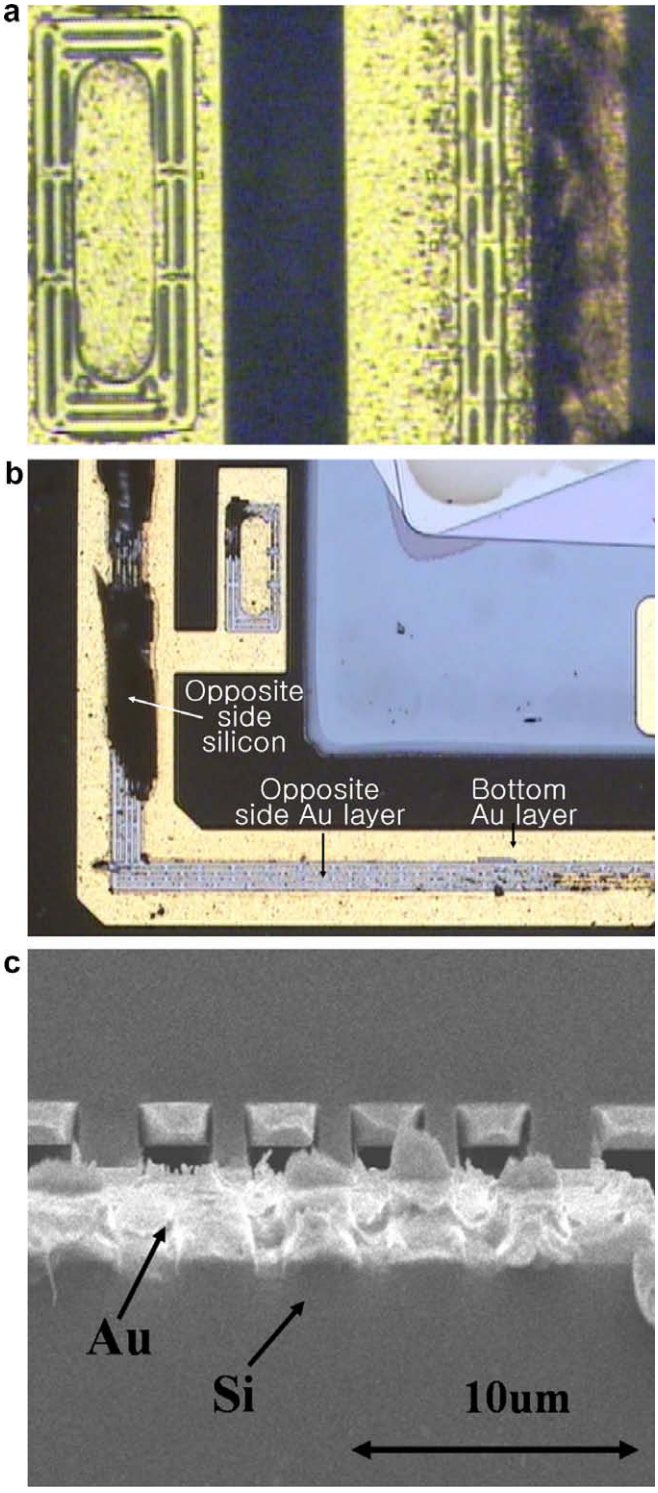

Fig. 4. Microscopy image of detached bonding test wafers: (a) only cap wafer marking is remained at the bottom of Au layer, and (b) the silicon with sealing layer was transferred to the bottom wafer.

rect bonding method can be a promising solution for a RF device applications.

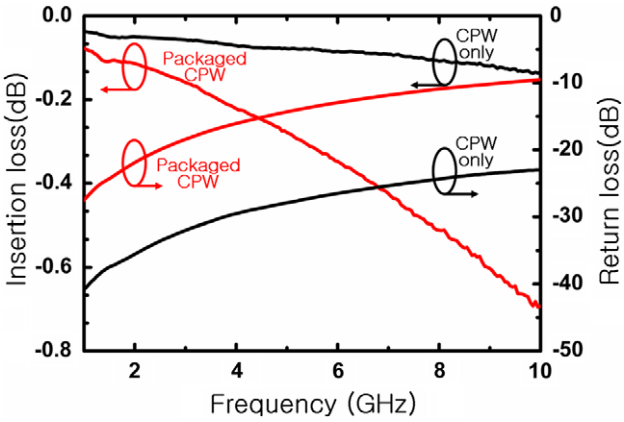

Fig. 5. Measured insertion loss of the packaged CPW line.

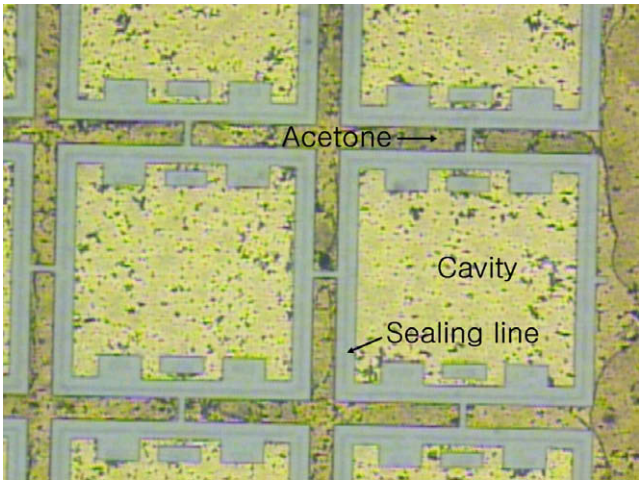

Fig. 6. Microscopy image of acetone dipped bonding test wafer: acetone permeated area is clearly distinguished with cavity area.

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