A zinc-oxide thin-film transistor using a spun-on dielectric and gate electrode

Jae-Hong Kwon *et al* 2009 *J. Phys. D: Appl. Phys.* **42** 065105 (6pp) doi: 10.1088/0022-3727/42/6/065105 Help

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Print publication: Issue 6 (21 March 2009)
Received 10 October 2008, in final form 31 January 2009
Published 3 March 2009

J. Phys. D: Appl. Phys. **42** (2009) 065105 (6pp) doi:10.1088/0022-3727/42/6/065105

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Received 10 October 2008, in final form 31 January 2009
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Online at stacks.iop.org/JPhysD/42/065105

Abstract
This paper presents an organic–inorganic hybrid transparent thin-film transistor (TTFT) with an active channel of zinc-oxide (ZnO). The solution-processed stagger type device consists of methyl-siloxane-based spin-on glass (SOG) and poly(3,4-ethylenedioxythiophene) : poly(styrenesulfonate) (PEDOT : PSS) for the dielectric and gate electrode, respectively. The TTFT, fabricated by this method, has an optical transmittance of 67.4%, and it displays a field effect mobility of 20.65 $cm^2\ V^{-1}\ s^{-1}$, an on/off ratio of $>10^4$, a threshold voltage of 6.9 V and a subthreshold swing of 1.02 V/decade when the drain voltage (V_{DS}) is 20 V.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Transparent electronics is currently one of the most advanced topics for a wide range of device applications that pervade our daily lives, being used as indispensable elements in a myriad of electronic products, such as photovoltaics, displays and home electronic appliances [1, 2]. Hence, transparent thin-film transistors (TTFTs) are key devices for realizing these transparent electronic products and the transistors have been fabricated on the basis of crystalline oxide channels that typically use a wurtzite structured zinc-oxide (ZnO) thin film as the active layer. Therefore, the devices have the virtues of being low cost, environmentally friendly and have especially high mobilities. Furthermore, ZnO has a number of outstanding characteristics, such as being a conducting oxide that is transparent, has a wide direct band gap (3.37 eV), a low dielectric constant, a large exciton binding energy (∼60 meV) and good photoelectric and piezoelectric properties [3]. Thus, ZnO has been studied for its potential use in many applications such as solar cells, sensors, transducers, light emitting diodes, diluted magnetic semiconductors, surface acoustic wave devices and infrared reflectors [4–10].

Recently, the growing interest in developing switching devices for portable invisible electronics has stipulated a requirement for thin-film transistors (TFTs) with high electronic performance, having optical transparency, being a simple and inexpensive process and a large area of coverage. Since TFTs meet all of the aforementioned requirements, and they are efficiently produced, many research groups have extensively studied unconventional materials and various processing strategies. For these reasons, unlike conventional semiconductor manufacturing flows, solution-based processes such as spin coating [11], spray coating [12], drop casting [13], screen-printing [14] and nanoimprinting lithography [15] are all very promising candidate methods for performing the manufacturing. This paper focuses on the construction and characteristics of the solution-process-based transparent inorganic–organic hybrid TFTs, and presents a discussion on the properties of ZnO-based TTFTs.

2. Experimental

This work describes the details of fabrication of new hybrid inorganic–organic TTFTs, utilizing indium tin oxide (ITO) for the source and drain electrodes, ZnO for the *n*-channel

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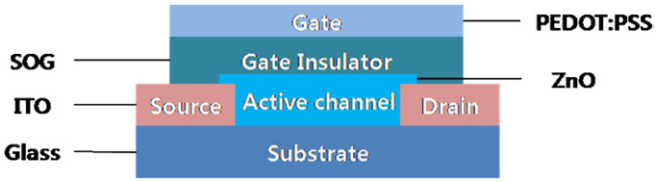

Figure 1. Schematic of the staggered TTFT structure on a glass with a top gate electrode.

active layer, methyl-siloxane-based spin-on glass (SOG, Honeywell 512B, dielectric constant $= 3.1 \pm 0.1$) for the dielectric and poly(3,4-ethylenedioxythiophene) : poly (styrenesulfonate) (PEDOT : PSS, PriMet-P, DPI Solution, Inc.) for the gate electrode. TTFT devices have a simple top-gate configuration that is fabricated onto a glass substrate, as shown in figure 1. The 100 nm thick source and drain contacts without intentional doping (with a channel width (W) of 12 mm and a channel length (L) of 700 μm) are defined by standard photolithography and lift-off techniques. A 200 nm thick channel layer is then deposited, by means of RF (13.56 MHz) magnetron sputtering, through a shadow mask, for the channel definition using 2.0 inch sputter targets, at a target-to-substrate distance of ∼6 cm, 100 W of power, a pressure of 20 mTorr and an Ar/O_2 ratio of 9 : 1. Next, the 650 nm thick SOG is spin coated, then baked successively at temperatures of 80 and 250 °C for 1 min at each temperature in air, and finally cured at 450 °C for 1 h at a 1.0 L min^{-1} N_2 flow rate. Finally, the ∼130 nm thick spin-coated PEDOT : PSS-based device is annealed using an oven at 120 °C for 30 min. Here, the gate dielectric is patterned after the gate electrode patterning; the gate electrode and dielectric are successively patterned by dry etching.

The surface and cross-sectional morphology is observed using a field emission scanning electron microscope (FE-SEM, Hitachi S-4300). The x-ray diffraction measurement (XRD, MXP3A-HF[22], MAC Science Co. Ltd, Tokyo) of the deposited ZnO film is performed to identify the resident phase of the film, to verify crystallite orientation and to evaluate the crystallite grain size. The surface morphology of the SiO_2, SOG and PEDOT : PSS layers is observed using scanning probe microscopy (SPM, XE-100 system, PSIA Inc.) The optical transmittances of all the deposited films are measured using an optical transmittance tool in the 200–800 nm wavelength range (Diode Array Spectrophotometer HP 8452A). Measurements of the film thickness are done by a surface profilometer (Tencor, Alpha-step 500) and the electronic characteristics of the devices are measured using a Keithley SCS/4200. All electrical measurements are performed in ambient air, at room temperature, in a dark box.

3. Results and discussion

Figure 2(a) shows the FE-SEM micrograph of the ZnO film morphology. This image reveals the polycrystalline structure with grain sizes of hundreds of nanometres, as shown in figure 2(b), which has a surface uniformity with a maximum value of the root mean square (RMS) roughness of 5.01 nm, and an average value of RMS roughness of 3.74 nm over

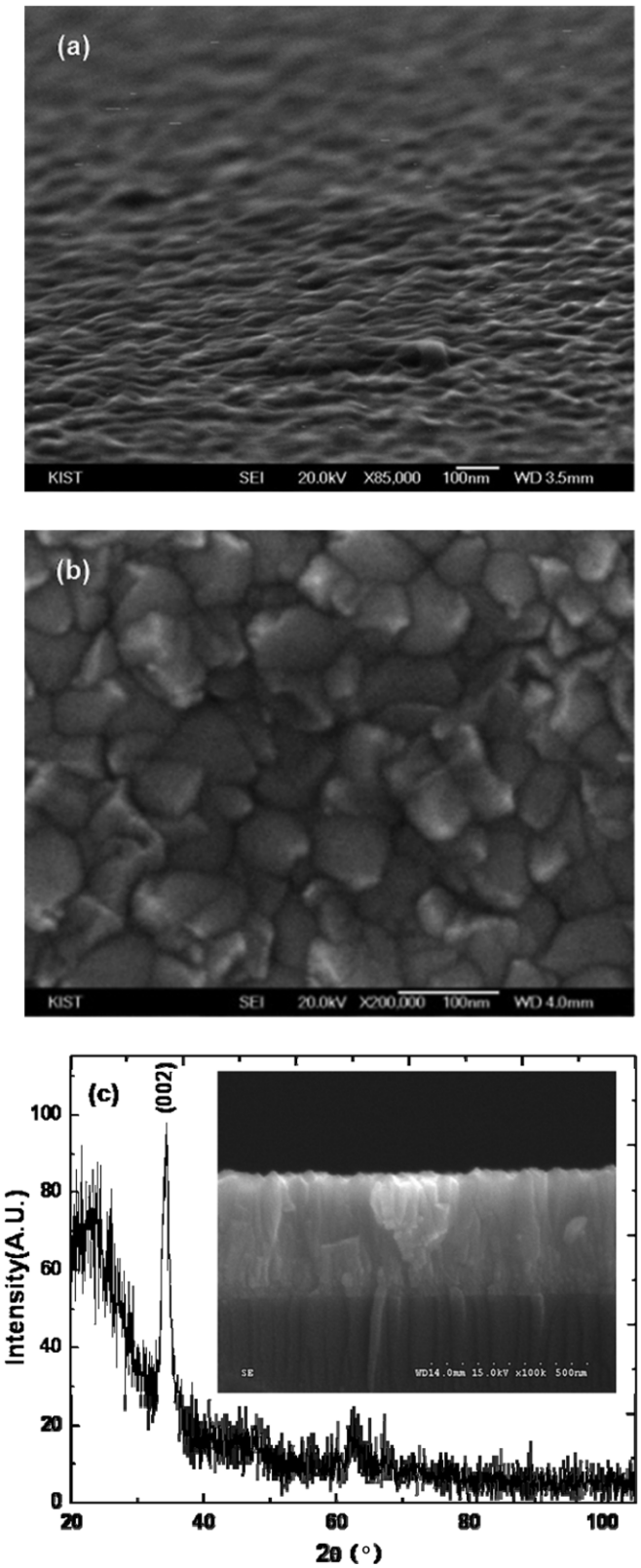

Figure 2. (a) An FE-SEM micrograph (with an apparent viewing angle of 16°) of the ZnO film. (b) An FE-SEM image of the ZnO surface film. (c) X-ray diffraction pattern of the ZnO film deposited on glass. The film thickness is 264 nm and the inset shows a cross-sectional FE-SEM image of the ZnO film.

a $1 \times 1\,\mu m^2$ area for all the sputtered films (not shown here). The smooth surface morphologies of the sputtered ZnO thin films can result in good interfaces of both the source and the drain electrode contacts with the ZnO channel layer, resulting in increased field effect mobility in the ZnO-based TTFT. In addition to the higher field effect mobility, other characteristics, such as the low off current and the low threshold voltage, are also suitable for using ZnO-based TTFTs as switching devices, which would extend the possibilities of high performance electronics. The inset of figure 2(*c*) shows a cross-sectional FE-SEM image of the ZnO film with regular and compact amassment grains vertical to the substrate. The x-ray spectra are shown in figure 2(*c*) for the sputtered ZnO film on a glass substrate (EAGLE 2000™ of Corning Inc.). The XRD pattern of the ZnO film exhibits an exclusive peak at 2θ 34.4°, which corresponds to the (0 0 2) peak of a hexagonal wurtzite structure of ZnO indicating that the preferential orientation of the *c*-axes of the crystallites is along the surface normal [16–21], which is also consistent with the results obtained from the FE-SEM images of figures 2(*a*) and (*b*). In addition, such results, and the presence of the *c*-axis orientation that is obtained in the ZnO films, demonstrate the availability of these properties for preferential semiconducting active channel layers [17–21].

The SOG is a well-known technology for the process of forming a dielectric layer between the metal lines in the low-cost fabrication of integrated circuits [22]. However, here, for a gate dielectric that can be processed in solution, a methyl-siloxane-based SOG, with a high optical quality of less than 10% of the wavelength of visible light (figure 5), is utilized. This SOG is composed primarily of siloxane that contains CH_3 (15% organic content) groups bonded to Si atoms in the Si-O backbone, which exhibits good uniformity, crack resistance, low stress, high thermal stability, chemical stability, good adhesion and a wide controlled thickness range [23–30]. Also, the local atomic concentration of the SOG using the energy dispersive x-ray analysis (EDX) has been previously reported [31]. The average atomic percentage ratio of O : Si has been measured and found to be 67.97 : 32.03, showing that the ratio of O to Si in the silicon oxide formed by the room-temperature reaction is 2.12. This is about the same as that of thermally grown SiO_2 (O/Si ratio of standard SiO_2: 2) [31].

Figure 3(*a*) shows a cross-sectional FE-SEM image of the SOG film on the pre-deposited ZnO layer, and it reveals a void-free, defect-free and well covered film. Figure 3(*b*) shows the SPM images of the SOG film where the bright areas in the images are interpreted as regions of increased film thickness and figure 3(*b*) is a topographic image of the SOG surface showing a very smooth surface with an RMS roughness of 0.18 nm over a $1 \times 1\,\mu m^2$ area. It is clearly seen that the surface film has no surface height differences, verifying that such a smooth surface is favourable for obtaining good performances. That is, the surface roughness of the gate dielectric film is a primary factor in obtaining high carrier mobility. If the dielectric film has poor surface roughness, then this roughness leads to valleys between the gate dielectric and the gate electrode. These valleys may act as carrier traps or scattering centres. Therefore, TTFTs that have a low surface

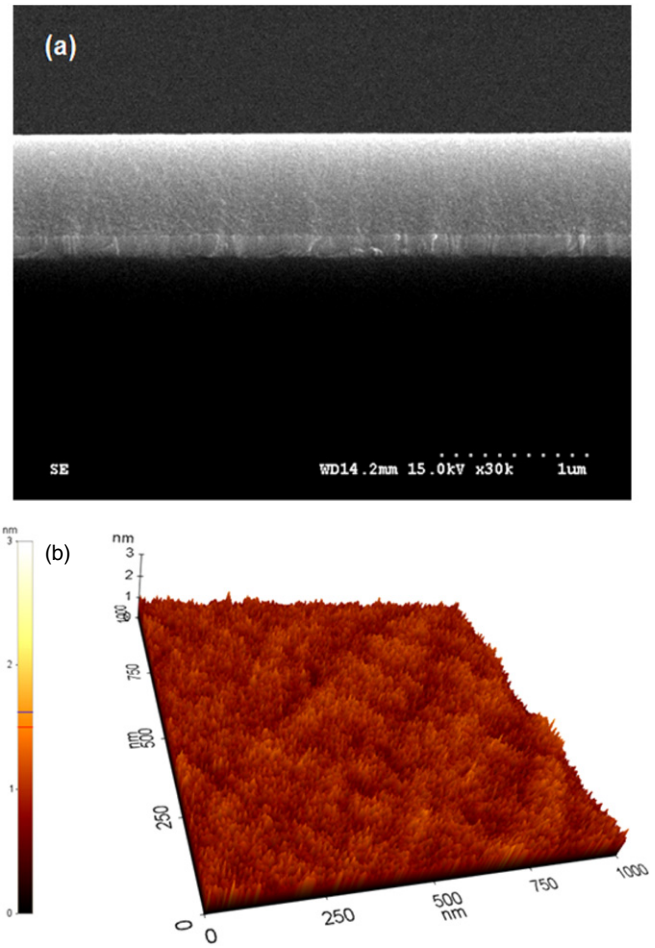

Figure 3. (*a*) A cross-sectional FE-SEM micrograph of the SOG film on the pre-deposited ZnO layer. (*b*) An SPM image (size $1 \times 1\,\mu m^2$).

roughness film exhibit good electronic performance. Also, it has already been confirmed that the surface roughness of SOG is smoother than that of thermally grown SiO_2 with an RMS roughness of 1.09 nm (not shown here).

Figure 4(*a*) shows a FE-SEM image of the spin-coated PEDOT : PSS layer, which has recently been used for application in organic devices [32]. Neutral PEDOT is difficult to process as it is insoluble and essentially intractable. In the doped form, PEDOT : PSS can be processed from aqueous colloidal dispersions, to give thin films of the quality required for applications in printed electronics [33]. Hence, a PEDOT : PSS is utilized as a spin-coated gate electrode that is transparent in the visible region of the spectrum (see figure 5). Figure 4(*a*) shows a tilted view FE-SEM image of the PEDOT : PSS surface morphology with many knoll-like shapes having diameters of ~1 μm. Figure 4(*b*) shows the SPM line profile along the line segment (blue line in figure 4(*a*)) of the PEDOT : PSS surface film that shows an irregular layer with an RMS roughness of 3.28 nm over a $1 \times 1\,\mu m^2$ area. Also, Ionescu-Zametti *et al* [34] have reported that the anisotropic surface morphology suggests that the polymer is organized into lamellar building blocks of an approximate thickness of 3 nm. Accordingly, the paracrystalline structure of PEDOT : PSS is explained by a layered structure, with PSS

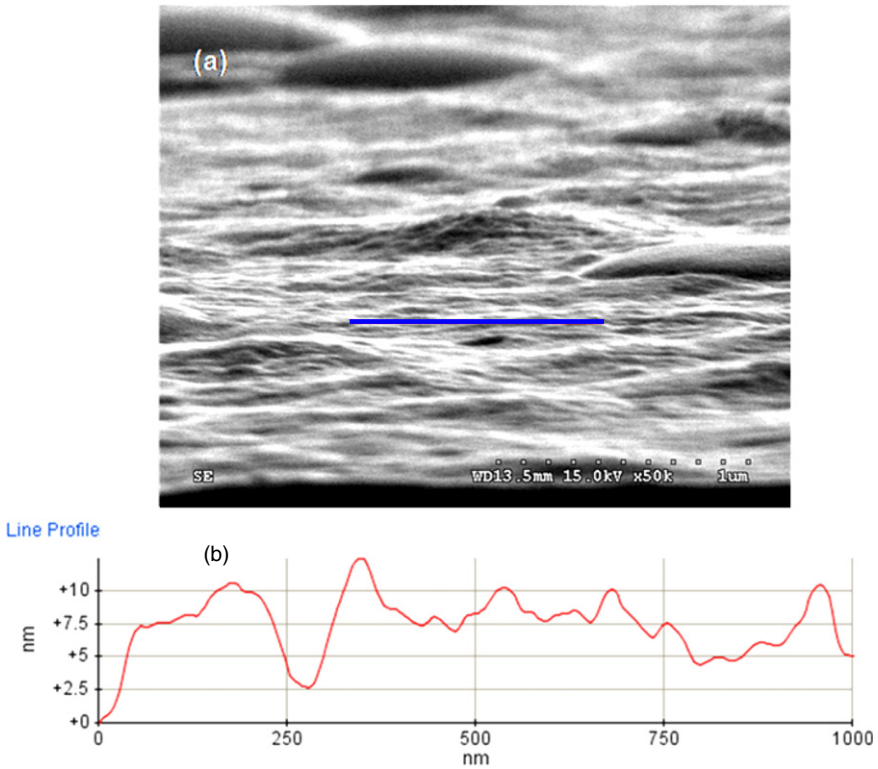

Figure 4. (*a*) An FE-SEM micrograph (with an apparent viewing angle of 8°) of the PEDOT : PSS film formed by spin coating. (*b*) An SPM line profile of the PEDOT : PSS surface film recorded along the blue/black line in (*a*). (Colour online.)

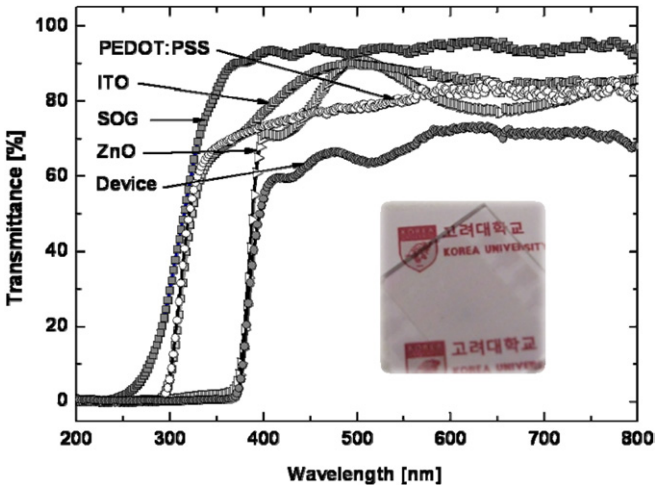

Figure 5. Plots of the measured optical transmission spectrum of the PEDOT : PSS film, the ITO film, the SOG film, the ZnO film and a ZnO-based TTFT in the wavelength range 200–800 nm. These films show average optical transmissions of 79.8%, 85.5%, 93.8%, 80.5% and 67.4%. The reference was obtained in air and the inset shows an image plan view of our TTFTs fabricated on a glass substrate placed on paper.

sandwiched between some of the PEDOT layers, giving it metallic properties.

Figure 5 shows the optical transmittance spectrum of the entire ZnO-based TTFT in the wavelength range between 200 and 800 nm (including the glass substrate), which includes the 100 nm thick ITO film (source/drain electrode), the 200 nm thick ZnO film (channel region), the 800 nm thick SOG film (gate dielectric) and the 130 nm thick PEDOT : PSS film (gate electrode). The average optical transmission of a ZnO-based TTFT, in the visible part of the spectrum (400–700 nm), is 67.4%, while at 550 nm it is 67.2%. The photo inserted in figure 5 shows a clearly visible $2 \times 2\,\mathrm{cm}^2$ glass substrate with ZnO-based TTFT devices.

The output and transfer characteristics are shown in figure 6 for ZnO-based transparent inorganic–organic hybrid TFTs using a spun-on dielectric (SOG) and a PEDOT : PSS gate electrode. Figures 6(*a*) and (*b*) show the corresponding transfer characteristics (drain current (I_D) versus gate voltage (V_G)) at drain voltages (V_DS) of 5, 10 and 20 V, for a ZnO-based TTFT, with a channel width (W)/length (L) of 16.43. The field effect mobilities are extracted from the saturation and linear regions of the transfer characteristics with the formula [35].

$$I_\mathrm{D}(\mathit{Linear}) = \frac{W\mu C_\mathrm{i} V_\mathrm{D}}{L}(V_\mathrm{G} - V_\mathrm{T}), \tag{1}$$

$$I_\mathrm{D}(\mathit{Saturation}) = \frac{W\mu C_\mathrm{i} V_\mathrm{D}}{2L}(V_\mathrm{G} - V_\mathrm{T})^2, \tag{2}$$

where $I_\mathrm{D}(\mathit{Linear})$ and $I_\mathrm{D}(\mathit{Saturation})$ are the drain current in the linear and saturation regions, W and L are the channel width and length, μ is the carrier mobility, V_T is the threshold voltage, C_i is the gate dielectric capacitance per unit area, $4.36 \times 10^{-5}\,\mathrm{F\,m^{-2}}$.

The proposed ZnO-based TTFT has field effect mobilities of both $20.65\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ in the saturation region (see figure 6(*a*) at $V_\mathrm{DS} = 20$ V) and both $5.12\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ in the linear region (see figure 6(*a*) at $V_\mathrm{DS} = 5$ V), and a drain current on/off ratio of more than 10^4. As figure 6(*a*) shows,

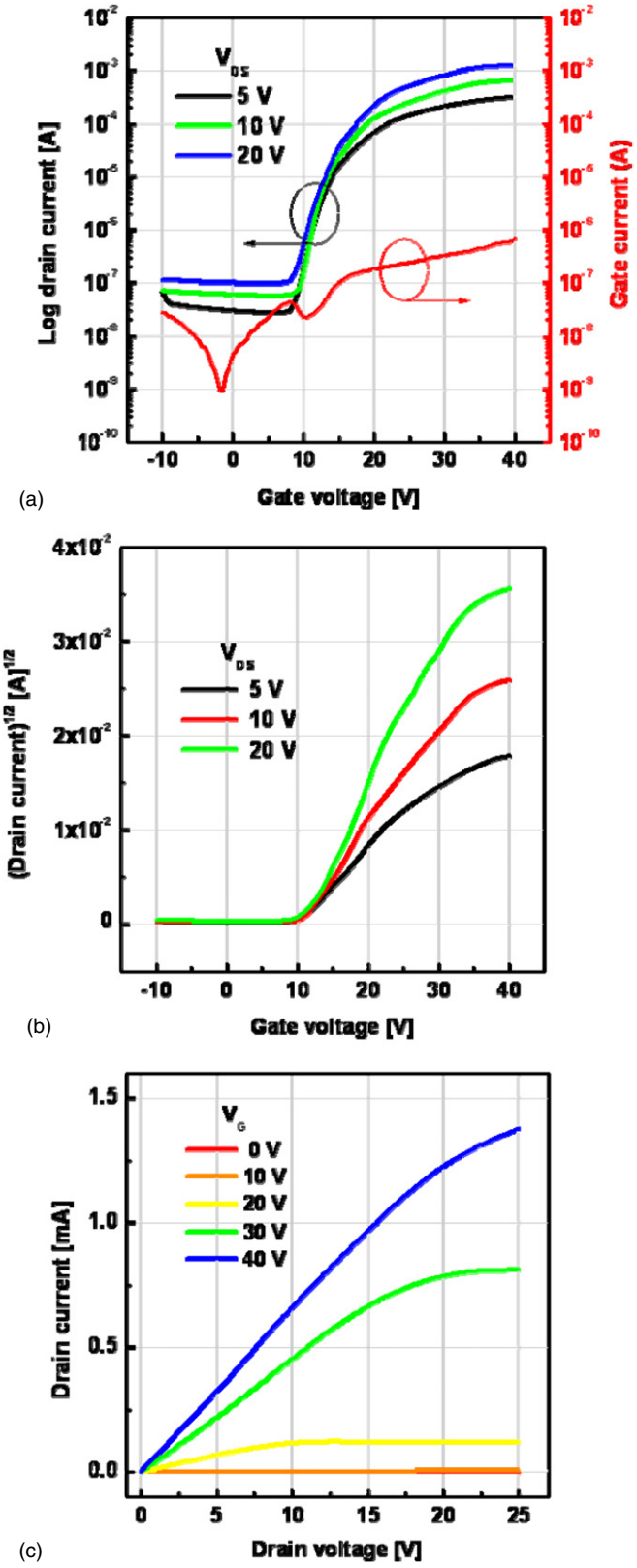

Figure 6. The current–voltage characteristics of a ZnO-based TTFT. (*a*) log I_D, (*b*) square root of the drain current ($\sqrt{I_D}$) as a function of V_G (from −10 to 40 V) at a drain to source voltage (V_{DS}) that varies between 5 and 20 V. (*c*) The drain current (I_D) versus the drain voltage (V_D) characteristics curve where the gate voltage (V_G) varies between 0 and 40 V in steps of 10 V.

the off current increases as V_{DS} increases, indicating that a bias dependence exists in the transfer characteristics of the ZnO-based TTFT. Also, the subthreshold slope is determined to be 1.02 V/decade from log I_D versus V_G (see figure 6(*a*)). Additionally, the gate leakage current of the proposed device is below 0.67 μA at maximum V_G, as shown in figure 6(*a*). The threshold voltage (V_T) is determined to be 6.9 V, from the corresponding plots of $\sqrt{I_D}$ versus V_G, showing that the ZnO-based TTFT operates in the enhancement mode, as shown in figure 6(*b*). In an enhancement-mode ZnO-based TTFT device, the channel conductivity increases with positive gate bias voltage, which is preferable for a TTFT being used as a switching device in electronic applications. Figure 6(*c*) shows I_D versus the drain voltage (V_D) for the ZnO-based TTFT at various gate voltages (V_G), which is a typical curve for *n*-type field effect transistors. The I_D–V_D characteristic exhibits pinch-off and current saturation. A minor current-crowding effect is observed at low drain voltages, and this effect is attributed to the relatively larger width [36] and length [37] of the active channel, compared with the devices reported in the literature [38]. Namely, the current-crowding effect is mainly caused by a high series resistance which can be attributed to the source/drain contact [39] and the series resistance of the channel, the latter of which increases as the channel width [40] or channel length [41] increases, which can be clearly seen in the fluent curve (i.e. linear regime) of the output characteristics at low V_D, wherein accumulated electron flows directly impact the electrical properties of TFTs, such as V_T, mobility, current on/off ratio and subthreshold swing. Perera and Krusius [42] have reported that the shallow doped source/drain contacts lead to the elimination of the current-crowding effect. However, from the experimental results, the proposed ZnO TTFT device is suitable for use as a switching device, which would extend the possibilities of high performance electronic applications.

4. Conclusion

To summarize, transparent electronics is an emerging technology whose objective is to produce invisible electronic circuits. This paper has described a new proposed fabrication of a ZnO-based TTFT, with a methyl-siloxane-based SOG, as the gate dielectric, and PEDOT : PSS as the organic gate electrode, and having the potential to simplify the processing of electronics has been demonstrated. In this work, the gate dielectric is patterned by a conventional photolithographic and dry etching process, and the gate electrode is patterned by dry etching. It is expected that the proposed method of fabricating devices will be applicable to other solution-processed electronics. The simplicity and low cost of the solution processing technique, as well as its adaptation to printed transparent electronics manufacturing, provide a very promising technology for industrial processes.

Acknowledgments

This work was supported by the National Research Laboratory (NRL, R0A-2007-000-20111-0) Program of the Ministry of Education, Science and Technology (Korea Science and

Engineering Foundation, KOSEF) and the KOSEF grant funded by the Korea Ministry of Education, Science and Technology (MEST) (No R11-2007-045-01003-0). We are indebted to Jong-Woo Lee (#1601 Venture Incubating Center, Hanwha Chemical R&D Center, Shinseong-dong, Yuseong-gu, Daejeon 305-345, Republic of Korea) for supplying the PEDOT : PSS. We also thank Young-Hoon Lee (GM DAEWOO R&D center, Cheongcheon-dong, Bupyeong-gu, Incheon 403-714, Republic of Korea) for the optical transmittance measurements.

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