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## Abstract

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# A flexible organic thin-film transistor with 6,13-bis(triisopropylsilylethynyl) pentacene and a methyl-siloxane-based dielectric

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ABSTRACT

In this paper, we describe our fabrication of a solution-processed organic thin-film transistor (OTFT) with 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) as the organic semiconductor (OSC) and methyl-siloxane-based spin-on glass (SOG) as the inorganic gate dielectric. Also, we compare these results with OTFTs using different substrates such as a silicon wafer or a polyethersulfone (PES) substrate. From electrical measurements, we observed exemplary *I–V* characteristics for these TFTs. We calculated the field effect mobility to be 0.007 $cm^2/V\,s$ for an OTFT fabricated on a wafer and 0.004 $cm^2/V\,s$ for an OTFT fabricated on a PES substrate.



## 1. Introduction

Organic thin-film transistors (OTFTs) have received considerable attention because they can be fabricated at reduced temperature with potentially reduced cost compared to hydrogenated amorphous silicon thin-film transistors (α-Si:H TFTs). Low fabrication temperature allows use in a wide range of applications such as RF identification tags, integrated circuits, electronic paper, and flat panel displays [1–4].

The vacuum-processed pentacene-based OTFT is particularly interesting as one of the most promising technologies. However, pentacene is not soluble in any convenient organic solvent, ruling out its use in solution processing. In addition, pentacene molecules are known to adopt a herringbone structure in the crystal so that their π–π overlap interactions are not optimized. Although pentacene, with its measured mobility values as high as 3 $cm^2/V\,s$ [5], is currently among the organic materials with the highest charge carrier motilities known, we believe that there still could be improvements in pentacene's mobility if its π–π interactions could be enhanced. Moreover, an optimized solution-processed pentacene-based OTFT using a flexible substrate enables a simple and non-vacuum fabrication of organic devices making possible extremely low-cost electronics that can be manufactured using printing techniques such as ink-jetting, nano-printing, and a roll-to-roll process [6].

In this research, we used a 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene, Hanafine Chem. Co.) as the organic semiconductor (OSC) for OTFT fabrication. By attaching a functional side group such as trimethylsilyl, triethylsilyl, triisopropylsilyl, *t*-btyl, hexyl and so on, research groups have made and further investigated soluble and stable functionalized pentacene [7–12]. Their work efforts have made standard fabrication methods such as solution processing more accessible for processing these materials into devices. Also, an important decision for the fabrication of OTFTs is the choice of the gate dielectric materials. Thus far, the best electrical performance for OTFTs has been obtained by employing high-quality inorganic gate dielectrics, such as thermally grown [13], sputtered [14], and chemical vapors deposited [15] insulators. However, these vacuum processes are not suitable for low-cost fabrication of OTFTs that have an attainable goal for use in inexpensive applications. Therefore, we utilized an inorganic gate dielectric that is spin coatable and methyl-siloxane-based spin-on glass (SOG, Honeywell 512B). SOG does not have the moisture and hysteresis problems of polymer dielectrics; it has a well planarized smooth surface roughness for a high mobility; and it has a lower dielectric constant (3.1 ± 0.1) and thus provides for better electrical insulation [16]. Therefore, it could replace the polymer dielectric as a gate insulator for OTFTs if it can be processed in solution and if its electrical properties are as good as or better than a polymer dielectric. In this paper, we discuss the re-

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sults we obtained for its optical properties and device performance in flexible electronic applications. This study can help us in understanding the structural relationships of the materials involved. It provides a useful guide for the rational design of transistor materials.

## 2. Experiments and results

For our studies, bottom-contact OTFT devices, as schematically shown in Fig. 1a and b, were fabricated using both an $n^+$ Si wafer (Resistivity 0.001–0.004 Ω cm) and a 200 nm-thick-indium tin oxide (ITO, sheet resistance 8.0–10.0 Ω/sq) on a 100 μm-thick-polyethersulfone (PES) film with the deposited SOG as the gate electrode and the gate insulator, respectively. Fig. 1c is a photograph of our completed device on a flexible substrate. An 800 nm-thick-SOG film was spin-coated and baked successively at 80 and 230 °C for 1 min each in air. Gold (Au, 200 nm thickness) source/drain contacts were deposited by electron-beam evaporation. Also, a shadow mask was used to define the source and drain electrodes. As shown in Fig. 1d, the channel width ($W$) and length ($L$) were 500 and 20 μm, respectively. Next, the TIPS-pentacene film was deposited by a drop casting. Finally, the coated TIPS-pentacene based devices were annealed using a hotplate at 110 °C for 2 min. After device fabrication, the transistor characteristics were measured using a Keithley SCS/4200 in ambient air.

The morphologies of TIPS-pentacene film were studied by using a scanning probe microscope (SPM, XE-100 system) technique. We interpreted the bright area in the image as an increase in the film thickness in that direction. Fig. 2a is a topographic image of the OSC film formed by drop casting from an 8 wt% solution of TIPS-pentacene in tetraline. The image illustrated that large crystals of TIPS-pentacene were grown directly on the SOG film (see Fig. 1e) and small crystals, which are estimated to be crystallized in the solution, was deposited on the large crystal with a root mean square (rms) roughness of 0.132 μm at 110 °C. Especially, this large surface roughness of TIPS-pentacene since drop-casted small-molecule OSC film leads to undesired randomly oriented crystalline domains within the film as shown in Fig. 1d and e, consequently giving a poor uniformity. These observations also suggest that further improved performance could be possible with more optimized processing.

To further investigate the molecular ordering in TIPS-pentacene film, we used X-ray diffraction (XRD, D/max 2200 V) spectroscopy in a symmetric reflection coupled $\theta-2\theta$ arrangement with a Cu $Ka_1$ radiation ($\alpha\lambda_{K\alpha 1}$ = 1.54 Å) X-ray source. Fig. 3 shows XRD results for an ~300 nm thick TIPS-pentacene thin film drop casted 8 wt% tetraline solution. The XRD result showed good molecular ordering for a solution deposited thin film and the same diffraction peaks as bulk crystal TIPS-pentacene [17–18]. Also, strong, sharp peak observed at 5.34° as shown in Fig. 3, indicated a well-organized molecular structure.

SOG is a well-known technology for the process of forming a dielectric layer between metal lines in low-cost fabrication of integrated circuits [19]. However, here, for a gate dielectric that can be processed in solution, we utilized SOG, composed primarily of siloxane which contained $CH_3$ (15% organic content) groups bonded to Si atoms in a Si–O backbone. The SOG exhibited good uniformity, crack resistance, low stress, high thermal stability, chemical stability, good adhesion, and a wide controlled thickness range [20–22]. Fig. 2b is a topographic image of the SOG surface on a silicon wafer showing a very smooth surface with rms roughness of 0.179 nm. Also, we confirmed SOG surface on an ITO-coated PES has likewise rms roughness of 0.223 nm (not shown here). We saw that the surface film was without any surface height difference. If the dielectric film has poor surface roughness, then this roughness leads to valleys in the channel region. These valleys may act as carrier traps with a number of scatterings [23].

We monitored the SOG film by Fourier transform IR (FTIR, JASCO FT-IR 320) spectroscopy as shown in Fig. 4. As shown in Fig. 4. The observed band at 2972 $cm^{-1}$ was assigned to the asymmetric, stretching vibrations of the methyl ($-CH_3$) groups. The 1273 $cm^{-1}$ band was assigned to Si–C stretching vibration. The 1011 $cm^{-1}$ peak was positive meaning that $SiO_2$ reconstructed to denser $SiO_2$ similar to thermally grown $SiO_2$ [24]. The 832 $cm^{-1}$, 799 $cm^{-1}$, and 770 $cm^{-1}$ peaks were assigned to the stretching vibrations of the Si–OH, Si–C, and Si–O, respectively [16]. We carried out elemental energy dispersive X-ray (EDX, Horiba EX-200) analysis (inset of Fig. 4) only for methyl-siloxane-based SOG. The

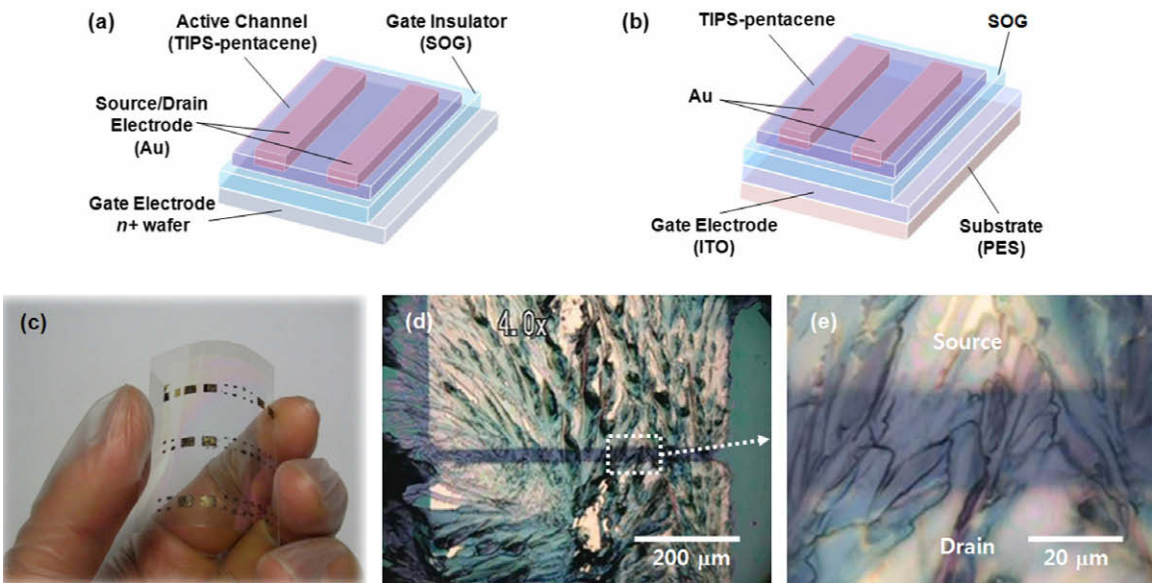


**Fig. 1.** A schematic diagram of an OTFT with bottom contact geometry (a) based on a flexible substrate and (b) based on a silicon wafer. (c) A photograph of our TIPS-pentacene and SOG-based OTFTs fabricated on a flexible PES substrate. (d) An optical micrograph of the OTFT. (e) An enlarged optical micrograph of the active channel of the OTFT along the rectangle line in Fig. 1d. The channel dimensions are $W/L$ = 25.

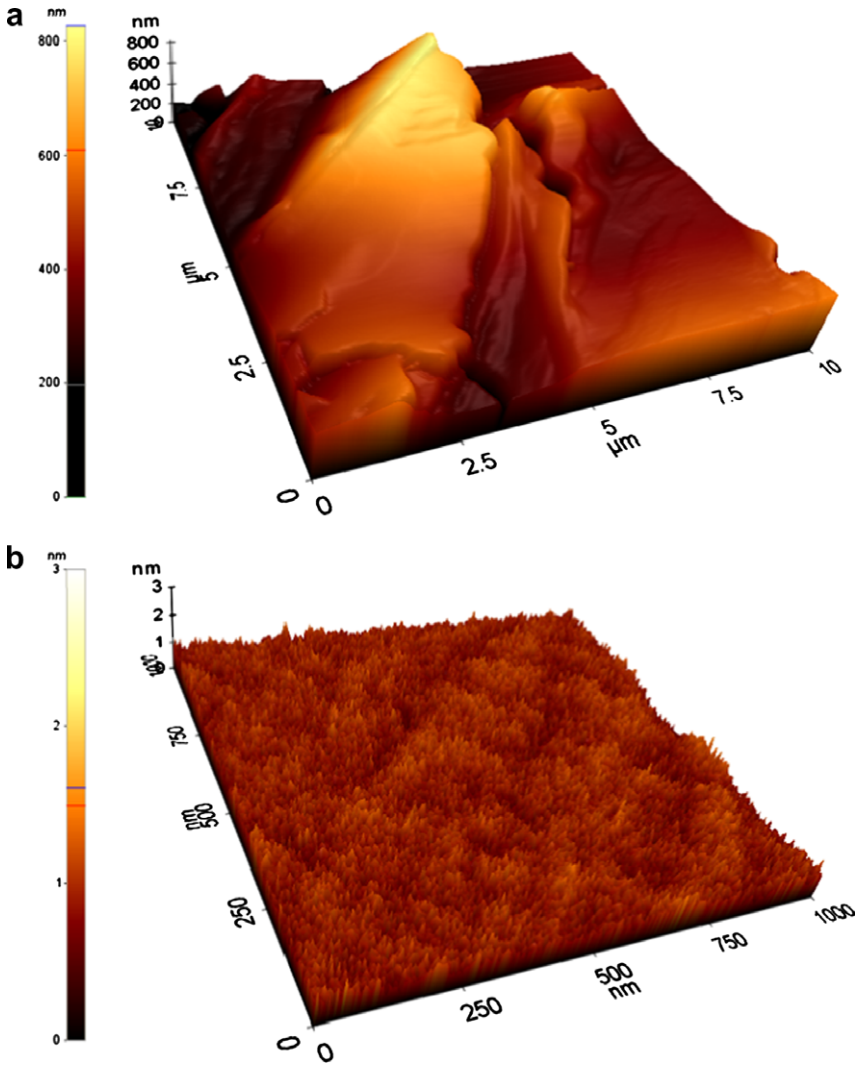


**Fig. 2.** SPM images of a drop-casted thin film TIPS-pentacene surface on SOG dielectrics and a spin-coated thin film SOG surface on a silicon wafer. (a) The morphology of drop-casted TIPS-pentacene film (rms roughness: 132.207 nm, scan size: $10 \times 10\ \mu m^2$). (b) The morphology of spun-on SOG film (rms roughness: 0.179 nm, scan size: $1 \times 1\ \mu m^2$).

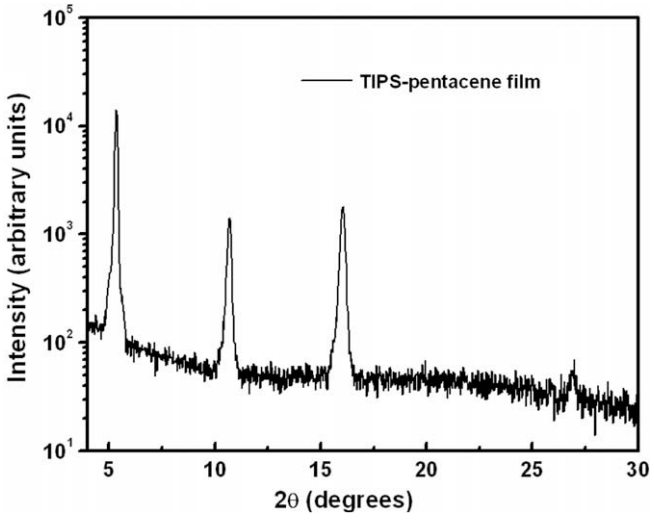


**Fig. 3.** An XRD spectroscopy result for drop-casted TIPS-pentacene film with an average thickness of 300 nm deposited on a glass substrate. The diffracting planes are parallel to the surface of the substrate.

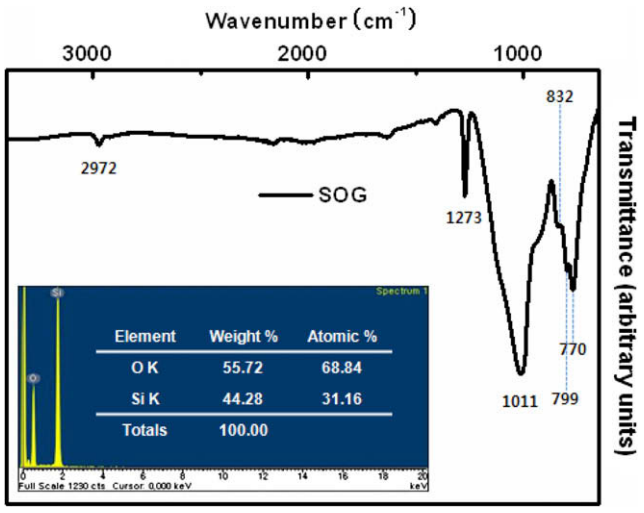


**Fig. 4.** FTIR spectra obtained from SOG film. The inset shows the EDX of a methyl-siloxane-based SOG film showing a stoichiometric elemental percentage analysis.

average atomic percentage ratio of O:Si was 68.84:31.16 (inset table of Fig. 4) showing that the ratio of O–Si in the silicon oxide, formed by the room-temperature reaction, was 2.20. This was about the same as that of thermally grown $SiO_2$ (O/Si ratio of standard $SiO_2$: 2) [25].

Fig. 5 shows the current voltage ($I$–$V$) characteristics of $p$-type OTFTs with a drop-casted a OSC and a spun-on gate dielectric on both a silicon wafer and a PES substrate. Fig. 5a and b show the drain current ($I_D$) versus drain voltage ($V_D$) of the OTFTs as the source–drain electrodes at different gate voltages ($V_G$) for OTFTs fabricated on a silicon wafer and on a PES substrate, respectively. The curves were typical for $p$-type material working in an accumulation mode. Output characteristics of the two devices revealed no noticeable contact resistance for OTFTs using different substrates as shown in Fig. 5a and b. However, the device characteristics varied substantially from one device to the next due to the variability of surface conditions. For example, the evaporation of an OSC droplet, induced an outward flow after the OSC drop-casted between metal lines, brought the solute towards the contact line and created a ring-like deposit after drying. This outward flow was a combination of the increased evaporation rate at the droplet edge and the contact line pinning caused by solute deposition near the edge. This phenomenon is known as the "coffee stain problem" [7,8,26,27]. On the other hand, to obtain an optimized condition for reliability of our devices, we observed OSC film deposition as a function of solvent, solution concentration, annealing times and temperatures, and other factors. The high work function of Au was expected to improve the injection of holes into the OSCs. The Au contacts sometimes produced low mobilities (<$10^{-3}$ $cm^2$/V s). The mobilities improved to about 0.007 $cm^2$/V s following annealing at a temperature of 110 °C for an OTFT fabricated on a silicon wafer (Fig. 5a); whereas an OTFT fabricated on a PES substrate produced a mobility of up to 0.004 $cm^2$/V s. The annealing may drive impurities away from the OSC and dielectric interface and increase the sizes of continuous crystalline domains, and/or improve the adhesion of the OSC to the dielectric. The corresponding plots of $Log\ I_D$ and $\sqrt{I_D}$ versus $V_G$, at a fixed drain voltage ($V_{DS}$) of −40 V for the devices, are shown in Fig. 5c and d. The subthreshold slope (SS) and current on/off ratio were determined and the field effect mobility ($\mu$) was extracted from $Log\ I_D$ vs. $V_G$. The threshold voltage ($V_T$) was determined from the corresponding plots of $\sqrt{I_D}$ versus $V_G$ listed along with our device characteristics in Table 1.

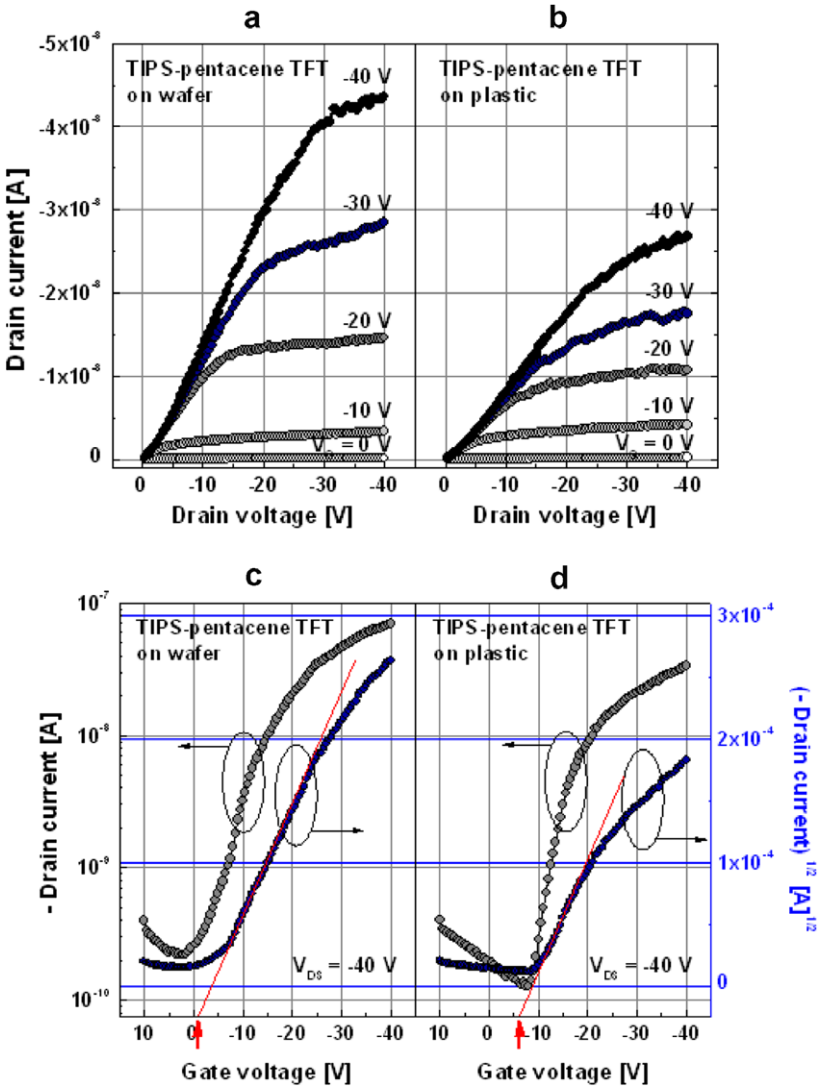


**Fig. 5.** Plots of the drain current ($I_D$) vs. the source–drain voltage ($V_{DS}$) as a function of gate voltage ($V_G$) obtained from TIPS-pentacene/SOG-based OTFTs fabricated on (a) a silicon wafer and (b) a PES substrate. The $Log\ I_D$ and square root of the drain current ($\sqrt{I_D}$) as a function of $V_G$ (from 10 V to −40 V) at $V_{DS}$ = −40 V obtained from TIPS-pentacene-based OTFTs fabricated on (c) a silicon wafer and (d) a PES substrate.

**Table 1**
OTFT parameters (field effect mobility, threshold voltage, current on/off ratio, and subthreshold slope) extracted from the transfer curves of OTFTs deposited on different substrates.

| Devices | $\mu$ ($cm^2$/V s) | $V_T$ (V) | On/off ratio | SS (V/decade) |
|---|---|---|---|---|
| OTFT on wafer | 0.007 | −1.0 | $3.16 \times 10^2$ | 1.30 |
| OTFT on plastic | 0.004 | −6.2 | $2.16 \times 10^2$ | 1.23 |

## 3. Conclusions

We fabricated flexible OTFTs with drop-casted OSCs, evaporated Au source–drain electrodes, spun-on gate dielectrics, and ITO-coated PES substrates. Moreover, we compared these OTFTs fabricated on Si wafers with OTFTs fabricated on PES substrates. We calculated the field effect mobility as 0.007 $cm^2$/V s for OTFTs fabricated on silicon wafers and 0.004 $cm^2$/V s for OTFTs fabricated on PES substrates. However, these characteristics are still insufficient to make good flexible electronics, so these devices need to be optimized by improving mobility to achieve the status of α-Si:H TFTs. In our work, the cost of OTFTs made by OSC coating is lower than pentacene-based OTFTs that need high-cost vacuum equipment. OTFTs made by OSC coating also might be compatible with low-cost processes such as inkjet, offset, nano-imprint, or roll-to-roll printing.

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