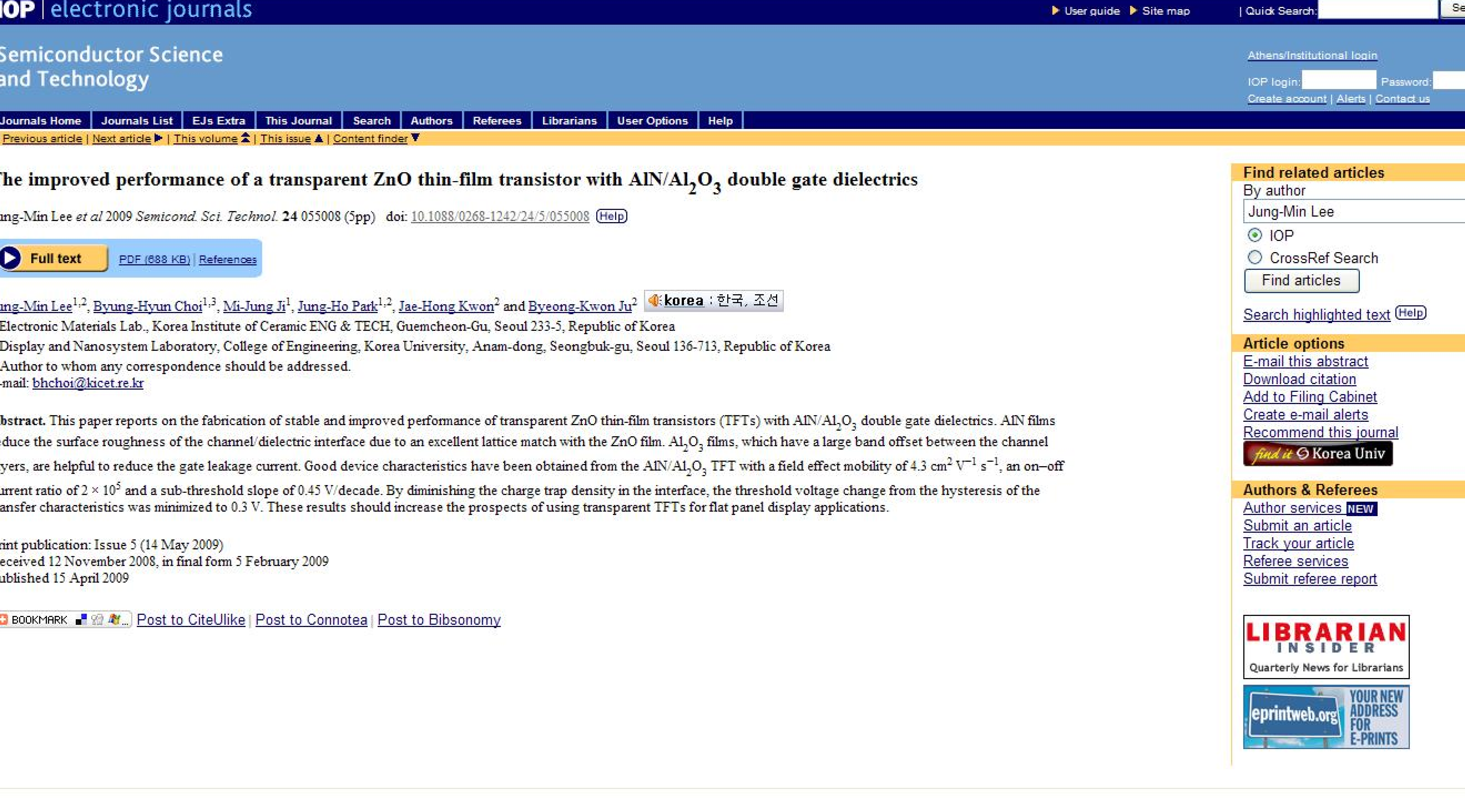

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The improved performance of a transparent ZnO thin-film transistor with AlN/Al_2O_3 double gate dielectrics

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Abstract. This paper reports on the fabrication of stable and improved performance of transparent ZnO thin-film transistors (TFTs) with AlN/Al_2O_3 double gate dielectrics. AlN films reduce the surface roughness of the channel/dielectric interface due to an excellent lattice match with the ZnO film. Al_2O_3 films, which have a large band offset between the channel layers, are helpful to reduce the gate leakage current. Good device characteristics have been obtained from the AlN/Al_2O_3 TFT with a field effect mobility of 4.3 $cm^2\,V^{-1}\,s^{-1}$, an on–off current ratio of 2×10^5 and a sub-threshold slope of 0.45 V/decade. By diminishing the charge trap density in the interface, the threshold voltage change from the hysteresis of the transfer characteristics was minimized to 0.3 V. These results should increase the prospects of using transparent TFTs for flat panel display applications.

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The improved performance of a transparent ZnO thin-film transistor with AlN/Al_2O_3 double gate dielectrics

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Abstract
This paper reports on the fabrication of stable and improved performance of transparent ZnO thin-film transistors (TFTs) with AlN/Al_2O_3 double gate dielectrics. AlN films reduce the surface roughness of the channel/dielectric interface due to an excellent lattice match with the ZnO film. Al_2O_3 films, which have a large band offset between the channel layers, are helpful to reduce the gate leakage current. Good device characteristics have been obtained from the AlN/Al_2O_3 TFT with a field effect mobility of 4.3 cm^2 V^{-1} s^{-1}, an on–off current ratio of 2 × 10^5 and a sub-threshold slope of 0.45 V/decade. By diminishing the charge trap density in the interface, the threshold voltage change from the hysteresis of the transfer characteristics was minimized to 0.3 V. These results should increase the prospects of using transparent TFTs for flat panel display applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The use of a transparent thin-film transistor (TTFT) is a key component for the next-generation displays and optoelectronic devices. Recently, applications of ZnO thin films have been studied intensively for their use as active channel layers of TTFTs in order to alternate conventional silicon or organic-based TFTs [1, 2]. This is because ZnO is transparent to the visible light region as a wide bandgap semiconductor (∼3.37 eV) as well as having a relatively high mobility and being able to be processed at low temperature [3]. So far, considerable efforts have been made to obtain high performance ZnO TFTs with high field effect mobilities (0.2–20 cm^2 V^{-1} s^{-1}) and on/off current ratios (10^4–10^7), and various gate dielectric materials (ATO, HfO_2, Al_2O_3, SiO_2, etc) have been used to decrease the leakage current and operating voltage [4–6]. However, there are several problems which currently hinder the manufacturability of ZnO TFTs as switching devices in display applications, namely the uniformity and stabilities of the device performances which are an important challenge that needs urgent investigation.

In a transistor, high interface trap density at the semiconductor–dielectric interfaces can increase the threshold voltage and the hysteresis characteristic. More often, a poor gate dielectric leads to excessive interface states and leakage current that is more limiting to the application. The quality of the interface and the dielectric also plays a significant role in specifying the stability of the transistor performances [7–9]. Therefore, there is a need to present the dielectric materials and their structures for realizing the highest performance transistors.

This paper describes a transparent ZnO thin-film transistor with an AlN/Al_2O_3 double gate insulator structure. The amorphous Al_2O_3 dielectric layers have been selected for their excellent dielectric properties and low gate leakage current due to its larger band offset, but the I_D–V_G hysteresis characteristics

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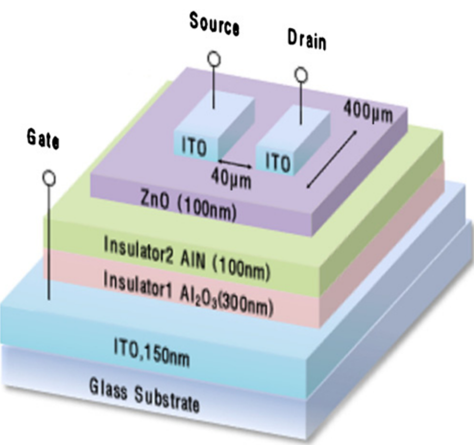

Figure 1. Schematic cross section of the ZnO TFT with the AlN/Al_2O_3 double gate dielectrics.

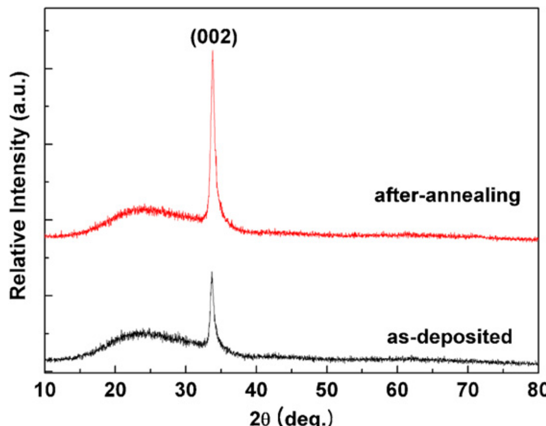

Figure 2. X-ray diffraction patterns of the as-deposited ZnO thin film and after annealing at 300 °C on a glass substrate.

have been observed from the ZnO TFT. Therefore, we introduce amorphous AlN which offers an excellent lattice match ($a = 3.1$ Å and $c = 4.98$ Å) with ZnO ($a = 3.2$ Å and $c = 5.2$ Å) than Al_2O_3 ($a = 4.75$ Å and $c = 12.99$ Å). Additionally, it is transparent to light and has a high dielectric strength (>20 kV mm^{-1}). By adopting the AlN/Al_2O_3 double dielectrics, enhanced device performance and small hysteresis can be obtained, suggesting a low trap density at the interface of the polycrystalline ZnO channel with the gate dielectric.

2. Experimental details

Figure 1 shows a schematic cross sectional view of transparent TFTs with double gate dielectrics which have an inverted staggered structure. The commercial indium tin oxide (ITO) coated glass was cleaned with acetone, methanol and deionized water, in that order. The ITO film on the glass substrate was used as the gate electrode and subsequently, the Al_2O_3 film was deposited as a gate dielectric layer via electron-beam (EB) evaporation using Al_2O_3 pellets (99.999%). The thickness of the deposited films was controlled using a quartz crystal thickness monitor to ensure a film thickness of 300 nm. In the case of the double gate dielectric structure, an AlN film of 100 nm was deposited on it by radio frequency (RF 13.56 MHz) magnetron sputtering using an AlN (99.99%) target. The sputtering was carried out at Ar and N_2 flow rates of 30 and 10 sccm (sccm denotes cubic centimeter per minute at STP), respectively, a working pressure of 30 mtorr and an RF power of 100 W. In order to use ZnO as the active channel layer, the background electron concentration of the ZnO thin film needs to be reduced [10] and this was attempted by mixing Ar and O_2 gas during the sputtering. An intrinsic ZnO channel layer of 100 nm was deposited by RF sputtering in Ar/O_2 with a flow rate of 36 sccm/4 sccm using the ZnO (99.999%) target and RF power of 100 W. Finally, the ITO source and drain electrode (150 nm) were deposited by RF sputtering in Ar (20 sccm) onto the ZnO layer using an ITO target (99.99%) with In_2O_3:SnO_2 (90 wt% and 10 wt%, respectively). The patterning of the source/drain electrode was performed by lift-off, and the channel width (W) and length (L) used were 400 and 40 μm, respectively. All the films were deposited at room temperature and a post-annealing of the fabricated TTFTs was performed at 300 °C in nitrogen for 60 min to increase the crystallinity of the intrinsic ZnO film and to enhance the conductivity of the ITO electrode.

3. Results and discussions

The structure properties of the ZnO films were determined using x-ray diffraction (XRD) measurements (Rigako D/MAX2200) with Cu Kα radiation. Figure 2 shows the XRD patterns of the as-deposited ZnO film and after annealing at 300 °C. They are all dominated by the 34° peaks, which correspond to the (0 0 2) plane of the hexagonal wurzite crystal structure and exhibit preferential orientation with the c-axis perpendicular to the substrate. Also, the XRD patterns exhibit the narrow full widths at half-maximum (FWHM) of the ZnO thin films after annealing. This result suggests that this film had good crystallinity and became close to stoichiometry with low structural defects and consequently higher resistivity [11].

The optical transmittance of the device was measured using a UV-VIS spectrometer (Simazu 2401). Figure 3 shows the optical transmittances of the structures indicated in the wavelength range between 300 and 800 nm (including the effects of the glass substrate). To investigate the relative contribution to the optical loss of each layer, the transmittances of the ZnO thin film on the glass substrate, Al_2O_3 TFT and AlN/Al_2O_3 TFT, have been measured. The average transmittances of the ZnO and TFT on the glass substrate have been found to be approximately 83% and 80%, respectively, in the visible region. The transmittances of the two devices are roughly analogous which indicates that transmittance losses due to the dielectric layer structure are negligible. The inset in figure 3 shows a clearly visible 2 cm × 2 cm glass substrate with the TTFT.

Atomic force microscopy (AFM, Digital Instruments dimension 3100) measurements were carried out in order

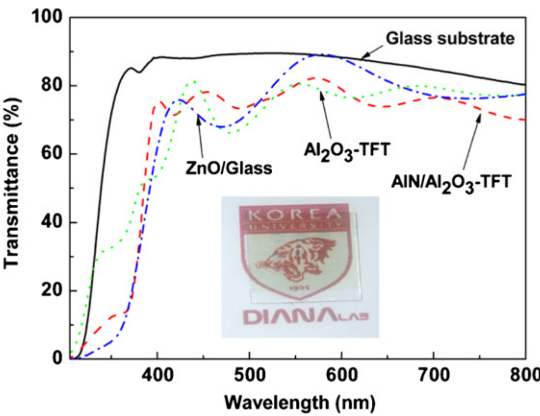

Figure 3. Optical transmittance spectra for the entire TTFT structure, including glass substrates. The inset shows a photograph of a 2 cm × 2 cm glass substrate with the ZnO TFT, placed on the text in the back.

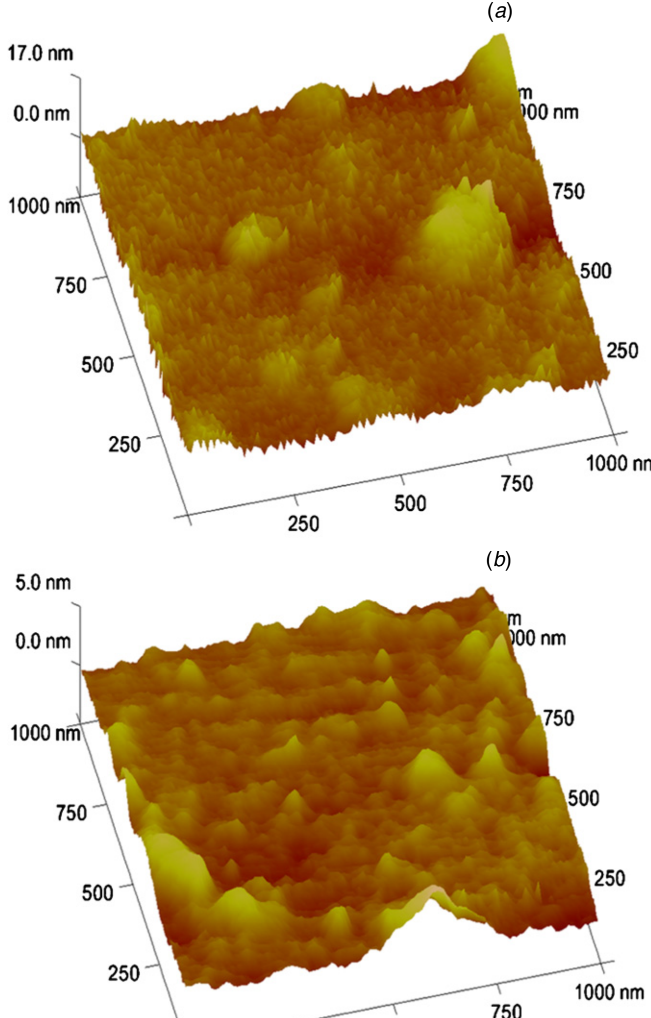

Figure 4. AFM images of the surface morphology of the ZnO film on the Al_2O_3 (*a*) and AlN/Al_2O_3 (*b*) gate dielectrics.

to investigate the surface morphology of the ZnO layer in the channel, and figure 4 shows the AFM images of the surface of the ZnO films on the Al_2O_3 and AlN/Al_2O_3 dielectrics. The surface roughness plays an important role in the performance of the devices and it has been found that the active channels with a smooth surface lead to better overall device performance, because a rough surface or interface may act as charge traps and scattering effects [12–14]. The root-mean-square (rms) roughness of the ZnO films on the Al_2O_3 layer was 1.82 nm, as shown in figure 4(*a*), which has been improved to 0.4 nm when the AlN dielectric film is deposited. These values demonstrate that the AlN film should be efficient due to a lower lattice mismatch with the ZnO films. It leads to smooth surface roughness through the improved local atomic rearrangement of the channel and dielectric interface by annealing.

All current–voltage (*I*–*V*) characteristics of the TTFTs were measured by the semiconductor characterization system (Keithley SCS 4200) in a dark box. Figure 5 shows the output and transfer characteristics of the Al_2O_3 and AlN/Al_2O_3 dielectric-based ZnO TTFTs. The output characteristics reveal that both devices operate as an n-channel enhancement mode and the Ohmic properties of the contact under low drain bias conditions. Also, these exhibit a complete pinch-off and hard saturation, as shown by the flatness of the I_{DS} curves for high V_{DS}. This indicates that the channel can be fully depleted of majority carriers (electrons) [11], and a maximum saturation current of 1.2×10^{-5} A was achieved under a gate bias (V_G) of 10 V from the AlN/Al_2O_3 TFT. The interfacial traps can additionally decrease the change in current resulting from a stepped increase in gate voltage, from the Al_2O_3 TFT. This effect is equivalent to a reduction in the transconductance of the TFT.

According to the transfer curve of figures 5(*c*) and (*d*), the on/off current ratios of the Al_2O_3 TFT and AlN/Al_2O_3 TFT are 4×10^4 and 2×10^5, respectively. The off-state leakage current is reduced in the AlN/Al_2O_3 TFT by at least an order of magnitude in value less than the off current (5×10^{-10} A) of the Al_2O_3 TFT. The saturation mobility (μ_{sat}) and the threshold voltage V_{TH} were calculated by linearly fitting the plot of the square root of the I_{DS} versus V_{GS} curve in the saturation region and applying the saturation region expression [15]:

$$I_{DS} = \left(\frac{C_i \mu_{sat} W}{2L}\right)(V_{GS} - V_{TH})^2 \text{ for } (V_{DS} > V_{GS} - V_{TH}), \quad (1)$$

where W is the channel width, L is the channel length and C_i is the capacitance per unit area of the gate insulator (around 18 and 14 nF cm^{-2} for the Al_2O_3 and AlN/Al_2O_3 dielectrics) The estimated μ_{sat} and V_{TH} were to be 2.6 and 4.3 cm^2 V^{-1} s^{-1}, and 6.2 and 4.8 V, respectively, for the Al_2O_3 TFT and AlN/Al_2O_3 TFT. These values are comparable to, or even exceed, those reported for intrinsic ZnO, conventional organic and a-Si:H TFTs [16, 17]. As evident from the transfer characteristics shown in figures 5(*c*) and (*d*), the turn-on voltage (V_{on}) of the TFT was about 4.9 and 1.6 V. Here, V_{on} is defined as the gate voltage at which the drain current begins to increase sharply.

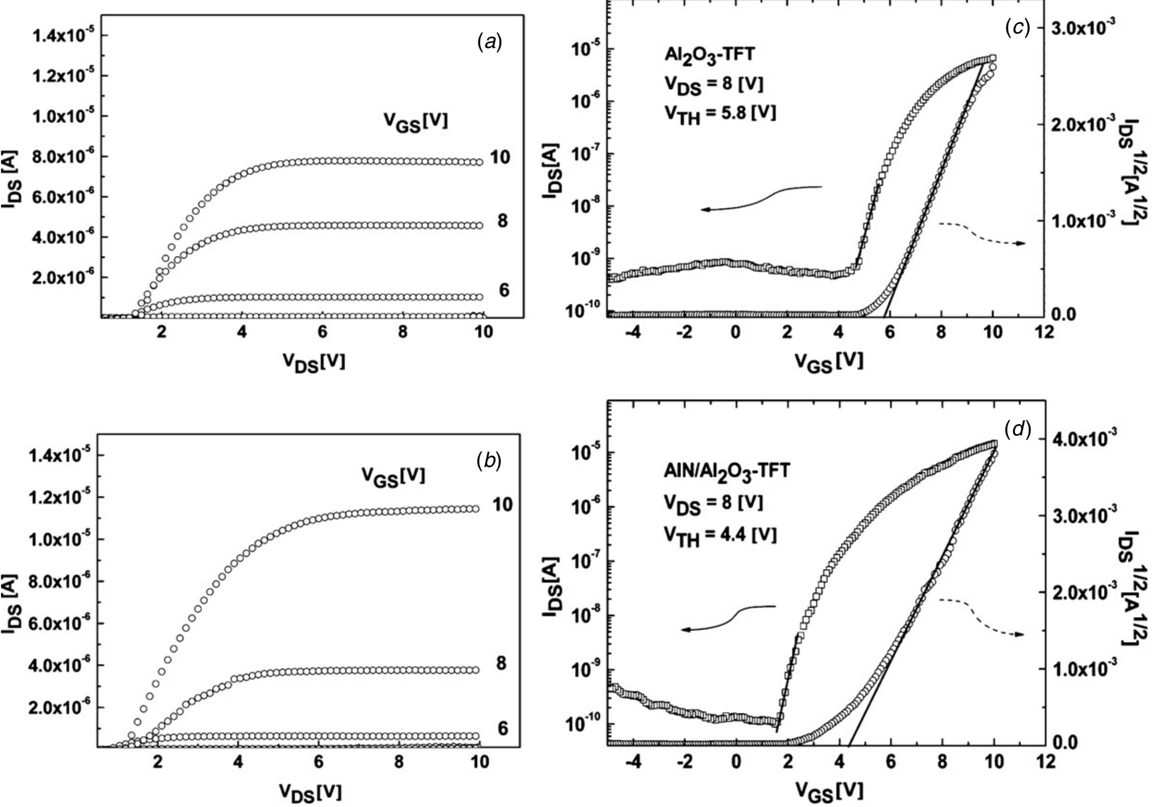

Figure 5. Typical output characteristics for the Al_2O_3 TFT (*a*) and the AlN/Al_2O_3 TFT (*b*). Transfer characteristics for the Al_2O_3 TFT (*c*) and the AlN/Al_2O_3 TFT (*d*).

From the transfer characteristics the sub-threshold slope, *S*, defined as the voltage required to increase the drain current by a factor of 10, can be determined as [15]

$$S = \frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}(\log I_{\mathrm{DS}})}, \quad (2)$$

where the sub-threshold slope was obtained as 0.45 and 0.6 V/decade, respectively, for the Al_2O_3 TFT and AlN/Al_2O_3 TFT. From *S* the maximum density of the interface state at the channel layer/dielectric interface can be inferred, and is given by equation (3) [15]:

$$N_t = \left(\frac{S\log(e)}{kT/q} - 1\right)\frac{C_i}{q}, \quad (3)$$

where k is Boltzmann's constant, T is the temperature and q is the electron charge. Indicative values of N_t are 1.0×10^{12} cm^{-2} for the Al_2O_3 TFT and 5.13×10^{11} cm^{-2} for the AlN/Al_2O_3 TFT. These results indicate that the AlN layer shows good performance as gate dielectric layers for the suppression of the charge trap at the channel/dielectric interface due to a superior lattice match with the ZnO film. Also, from the AFM results of figure 4(*a*), the rough interface prohibits the transport of accumulated electrons and increases the scattering, leading to low field-effect mobility, low saturation drain current and high threshold voltage.

A hysteresis effect was observed in the forward and reverse voltage sweeps for the transfer curve for the Al_2O_3 TFT and the AlN/Al_2O_3 TFT. The clockwise hysteresis is caused by accumulated electrons at the channel/dielectrics interface during the forward sweep of the gate voltage [18]. The threshold voltage change of the AlN/Al_2O_3 TFT from the hysteresis was 0.4 V smaller than that of the Al_2O_3 TFT, as indicated in figure 6. The width of hysteresis was suppressed, indicating improved channel/dielectric interface characteristics. Also, the reduced hysteresis in TFTs may be attributed to the oxygen content of the ZnO film during the sputtering [19].

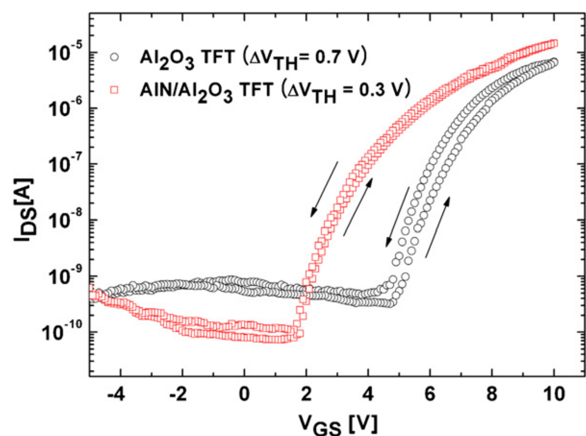

Figure 6. Hysteresis in the transfer curve corresponding to drain current responses to gate voltage sweeps from −5 V to 10 V and back to −5 V.

4. Conclusions

Transparent ZnO TFTs have been fabricated with an Al_2O_3 single dielectric layer and an AlN/Al_2O_3 double dielectric layer. The Al_2O_3 dielectrics contribute to reducing the gate leakage current due to its large band offset between the channel layers. The ZnO TFTs with double dielectric layers have been found to exhibit significantly improved behavior in their overall electrical characteristics. The threshold voltage change from the hysteresis of the transfer characteristics was minimized as 0.3 V. It has been demonstrated that the use of the AlN dielectrics lead to smoother interfaces in comparison to Al_2O_3, which reduce charge trapping at the interface and scattering effects. It is expected that the proposed AlN/Al_2O_3-TFT devices will be useful to further advance the TTFT technology for future display applications.

Acknowledgments

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