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This work reports on the fabrication of organic thin-film transistors (OTFTs) with a solution-based 6,13-bis(triisopropylsilylethynyl) pentacene by a drop-casting method, and the determination of the electrical properties of OTFTs having different source/drain

Hysteresis Effects by Source/Drain Interdigitated-Finger Geometry in 6,13-Bis(triisopropylsilylethynyl)pentacene Thin-Film Transistors

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This work reports on the fabrication of organic thin-film transistors (OTFTs) with a solution-based 6,13-bis(triisopropylsilylethynyl)pentacene by a drop-casting method, and the determination of the electrical properties of OTFTs having different source/drain interdigitated-finger electrodes. The results show that the hysteresis in transfer characteristics of the OTFTs depends on the variation of contact fingers. These hystereses lead to changes in threshold voltage, which originates from charge trapping/detrapping at or near the organic semiconductor/dielectric interface. These related phenomena also influence the device parameters such as the field-effect mobility, the on/off current ratio, and the gate current.
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Organic thin-film transistors (OTFTs) are now being investigated due to their potential advantages including easy processing, simple structure, and low process temperature, all of which provide good compatibility with plastic substrates. Recently many research groups have successfully demonstrated numerous OTFT-driven devices, such as liquid-crystal displays,[1] organic light-emitting diodes,[2] and electronic papers.[3] These technologies have received considerable attention recently because solution processability enables a low cost fabrication process such as spin coating,[4] drop casting,[5] screen printing,[6] and spray coating[7] for large areas.

The position aberration of the transistors or the variation in the source–drain geometries (channel width W or channel length L and source–drain electrode shapes defined by nonrectangular or rectangular types) significantly affects the pixel-driving properties of the transistors, which results in the deterioration of the display performances. Therefore, it is important for the channel geometry, where the channel is substantially under the pixel electrode, to be considered at the design stages.

OTFTs can have channels defined by their source–drain interdigitated fingers (SDIFs) on the drain and pixel electrodes, giving a larger W/L if the OTFT resided only along one or more edges of the pixel. SDIF designs are advantageous because they allow for maintaining a larger W/L ratio with a larger L than for an OTFT constrained to only being able to lie adjacent to the pixel electrode. This permits the use of printing and other techniques, for fabricating display back-planes that are not capable of attaining the fine-resolution limits of standard silicon processing using photolithography. Also, SDIF designs enable the achievement of larger W and L without reducing the aperture ratio of the display.[8]

This article focuses on the study of the electrical characteristics of solution-processed OTFTs made from 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) mixed with poly(4-vinylbiphenyl) (PVBP) with varying number of SDIF electrodes for achieving high device performances.

Experimental and Results

Figure 1a shows a schematic of the OTFT structures with varying SDIF-type electrodes such as four-fingered, three-fingered, and two-fingered electrodes and without any SDIF (zero-finger) electrode. All devices contain an insulator layer of silicon dioxide (100 nm) which is thermally grown on top of a highly doped p^{++} silicon wafer to act as the gate contact. A 200 nm thick source–drain Au contact was fabricated on top of the insulator by a thermal
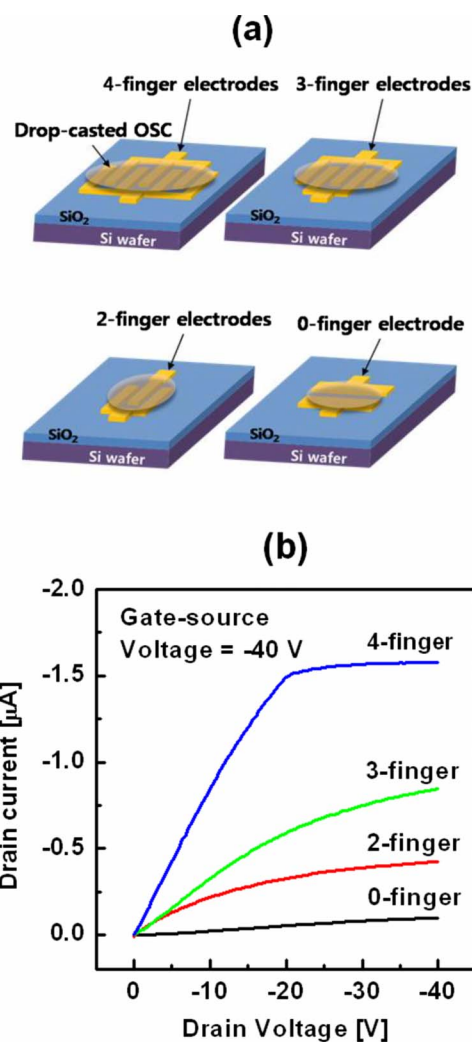

Figure 1. (Color online) (a) Device structures of OTFTs with channel width/length (W/L = 2500 μm/100 μm) and four types of SDIF bottom contacts: four-, three-, two-, and zero-finger electrodes. (b) SDIF-type electrode dependence of I_D in OTFTs at V_{GS} = −40 V.
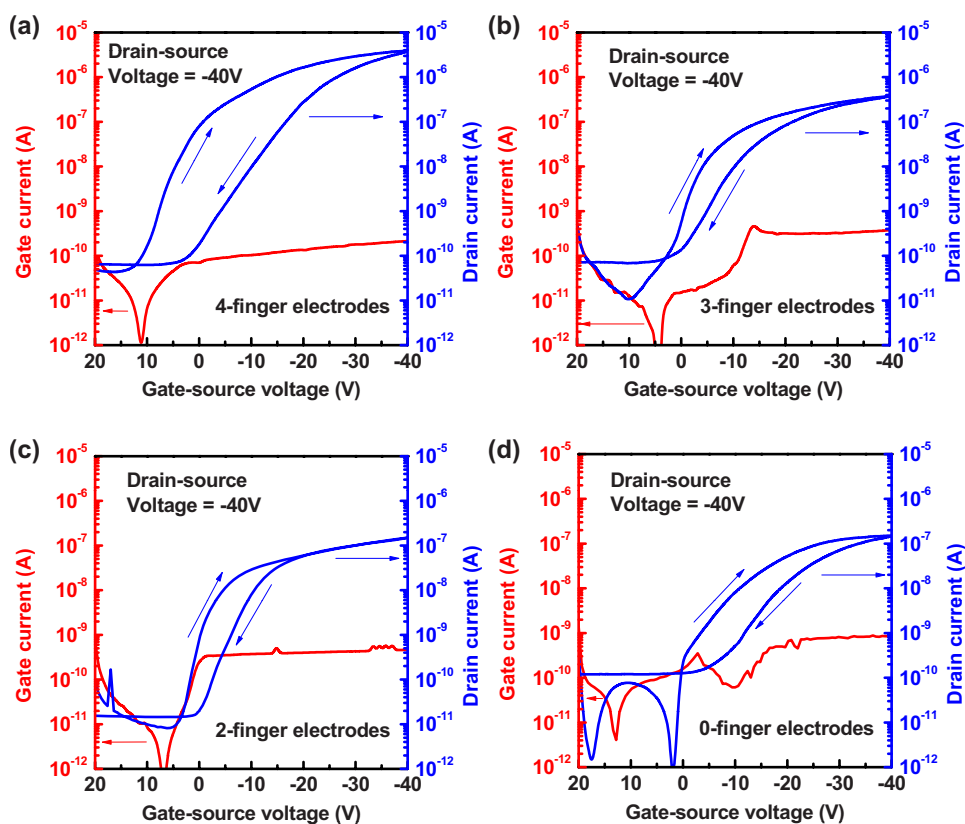
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Figure 2. (Color online) Plot of drain current (I_D) and gate current (I_G) as a function of gate–source voltage (V_{GS}) for interdigitated (a) four-finger, (b) three-finger, (c) two-finger, and (d) zero-finger electrodes at drain–source voltage (V_{DS}) = −40 V.

evaporation method (DOV Co., Ltd) to give a width W of 2500 μm and a length L of 100 μm using a shadow mask. The TIPS-pentacene mixed with PVBP (Sigma-Aldrich, used as-received) was deposited by drop casting from a 2 wt % solution of TIPS-pentacene in monochlorobenzene. Here, the polymer binder, PVBP, uniformly improved the film formation over a large area and helped the TIPS-pentacene to form a good film quality on the dielectric layer to provide the function of forming a good interfacial contact between the source/drain electrodes onto the active channel layer.[9-12] Finally, after coating the active layer, the device was annealed using a hot-plate at 110°C for 1 min. After fabrication of the device, the transistor characteristics were measured using an Agilent 4156C controlled by Labview.[13]

Figure 1b shows the drain current (I_D) vs the drain voltage (V_D) at a constant gate–source voltage (V_{GS}) of −40 V, measured from four differently prepared OTFTs. These devices showed a typical p-type OTFT working in accumulation mode, namely, the presence of a linear regime at $|V_D| < |V_{GS}|$ followed by a saturation regime at $|V_D| > |V_{GS}|$. It is clearly seen that I_D has been improved with the increase in the number of SDIFs confirming the typical characteristics of the field-effect transistors. The saturation I_D of the OTFT with four fingers is ~16 times larger to that without the SDIF electrode; in fact the maximum drain currents (i.e., I_D at V_{GS} = V_D = −40 V) were 0.1 μA for the zero-finger geometry, 0.4 μA for the two-finger geometry, 0.8 μA for the three-finger geometry, and 1.6 μA for the four-finger geometry. The device with four fingers leads to a significantly increased I_D and an enlarged slope than other devices with electrode geometries with/without SDIF electrodes in the linear region of the I_D-V_D characteristics. The slope of the linear region reflects the total device resistance of the transistor, which is composed of the channel resistance and the parasitic resistance. This total resistance is mainly influenced by the contact resistance, especially by the coupling between the contacts and the transistor channel.[14-16] Therefore, these devices with SDIF electrodes may provide smaller total device resistance as the number of SDIFs increases, as shown in Fig. 1b.

Figure 2 shows the transfer characteristics of devices with and without SDIF electrodes, which were swept in both directions. The drain current value $|I_D|$ of the off-to-on curve is larger than that of the on-to-off curve. Hysteresis of this loop direction has always been observed for OTFTs using a thermal SiO_2 dielectric as it is dominated by long-lifetime deep charge traps in the organic semiconductor (OSC) or at the interface.[17] This clearly shows that the phenomenon of the reduced hysteresis properties decreased with the number of SDIF electrodes. The device with two fingers, seen in Fig. 2c, shows less hysteresis than that with four fingers shown in Fig. 2a, which also has more hysteresis than that seen in Fig. 2b. The different hysteresis phenomenon caused by employing different SDIF electrode types is attributed to differences in the quantities of charges trapped at the interface between the SiO_2 and the OSC layers. The device with four fingers from Fig. 2a, in particular, shows much more hysteresis than the devices in Fig. 2b and c. This could possibly be because of the larger overlap area covered with the SDIF geometries, which determine the storage capacitance[18]

$$Q = \varepsilon_r \varepsilon_0 A V / d \qquad [1]$$

where Q, ε_r, ε_0, A, V, and d are the quantity of electric charge, the relative static permittivity, the permittivity of free space, the covered area between OSC and dielectric layer, the applied voltage, and the separation between the gate and source/drain electrodes, individually. Based on Eq. 1, a larger A leads to a larger Q because of more charge to be stored in the insulator both above and below the OSC (i.e., A is directly proportional to Q).

The device parameters are identified as the on-current (I_{on}), the off-current (I_{off}), the on/off current ratio ($I_{on/off}$), and the gate current (I_G) as a function of the number of fingers. It can be seen in Fig. 3a that as the number of fingers increase, both I_{on} and I_{off} are increased. Because the increase in I_{on} is greater, an increase in $I_{on/off}$ was also observed. The generation of I_{off} is especially attributed to the thermionic emission at a low electric field and the field-enhanced emission at a high electric field.[19] Hence, the magnitude of the electrical field and the amount of traps within the drain depletion region
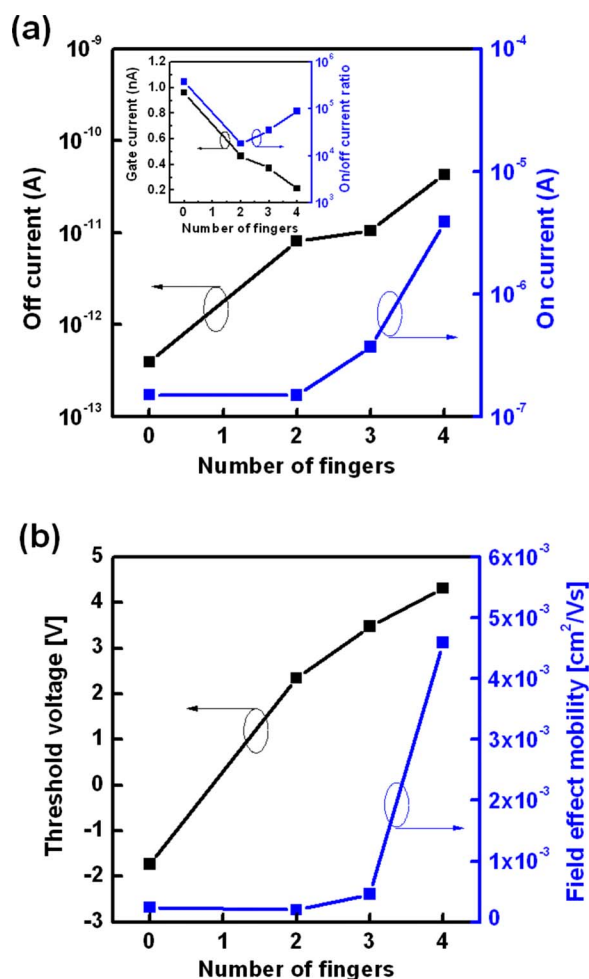
Figure 3. (Color online) (a) Number of fingers vs the off-current and the on-current (the inset shows a comparison of the gate current and the on/off-current ratio at different SDIFs). (b) Variation in the threshold voltage and the saturation mobility for different SDIF electrodes in OTFTs.

cause the variations in I_{off}, which are also associated with the amount of defects or traps in the drain depletion region.[20] Thus, with the increasing number of fingers, the increase in the density of fixed charges at the active channel/dielectric interface[21] and the increment of the local electric field in the drain depletion region lead to the marked increase in I_{off}.[20] Also, I_G (i.e., $V_G = V_D = -40$ V), which was due to leakage between the source and gate electrodes through the gate insulator, is reduced as the number of SDIF electrodes is increased, as shown in the inset of Fig. 3a. This property is due to the increase of the lateral electric field along the channel toward the drain[22] as the number of contact fingers increases.

Figure 3b shows a plot of the field-effect mobility (μ) and the threshold voltage (V_T) at $V_G = -40$ V as a function of the number of fingers. As the number of fingers is increased from 0 to 4, there is an increase in μ from 2.4×10^{-4} to 4.6×10^{-3} cm²/V s while V_T increases from -1.73 to 4.31 V. Here, μ shows considerably greater increase for the device with four fingers than for the other devices due to the improved carrier transportation. Meanwhile, deep charges trapped (Q_d) in the channel bring about the variation of V_T. More-

over, V_T is a measurement of the surface density of Q_d in the channel. The relationship between these is shown in the following equation[23]

$$V_T \approx Q_d/C_i \qquad [2]$$

where C_i is the capacitance per unit area of the SiO₂ layer. From Eq. 2, the density of Q_d by the generated charge trap may result in the alleviated V_T with large hysteresis characteristics.

Conclusion

In summary, solution-processed OTFTs have been fabricated, their electrical characteristics studied, and the effects of various source–drain electrode geometries, with and without SDIFs, have been investigated. By employing the SDIF structure, the following aspects have been clarified: Decrease in the total resistance of the transistor, enhancement of the μ, and reduction of the I_G as the number of SDIF electrodes increase. With increasing number of SDIF electrodes, the charge trappings are increased, causing a larger hysteresis, which also increases the V_T and the I_{off}.

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