Thick-membrane-operated radio frequency switches with wafer-level package using gold compressive bonding

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Abstract. An electrostatically actuated radio frequency (rf) switch is fabricated using a thick silicon membrane, and the device is packaged using a high resistivity silicon cap wafer with a gold (Au) thermocompressive bonding method. To achieve an rf switch that can operate at low voltage, a thick membrane with a pivot under the membrane is used. This design makes it possible to maintain the very small gap between the electrodes and the membrane without bending. A cavity with a pivot-patterned silicon wafer and a coplanar waveguide (CPW) signal-line-formed glass wafer is bonded using an anodic bonding method. After a mechanical polishing process, a deep reactive ion etcher is used to fabricate the membrane structure with a spring and a spring bar. To package the fabricated rf switch, an Au thermocompressive bonding process is used. A 1-μm-thick sputtered Au layer is used as intermediate bonding material. The bonding temperature and pressure are 350 °C and 63 MPa, respectively, and the time duration of the bonding is set to 30 min. The electrodes of the switch and the electrical contact pads on the cap wafers are interconnected via a hole and a sputtered Au metal layer. The total size of the complete packaged rf switch is 2.2 × 1.85 mm, and its rf characteristics have been measured using a Hewlett−Packard (HP) 8510C network analyzer. The measured driving voltage is approximately 16 V, the isolation is approximately −38.4 dB, and the insertion loss is approximately −0.43 dB at 2 GHz. *© 2009 Society of Photo-Optical Instrumentation Engineers.* [DOI: 10.1117/1.3238545]

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1 Introduction

P-i-N diodes, junction field effect transistor (JFET), and GaAs Metal semiconductor field effect transistor (MESFET) switches are widely used in rf circuits because of their compact size, low manufacturing cost, and compatibility with other rf modules. However, when used in wideband or high frequency communication systems, the rf performances of these switches decrease dramatically. This performance degradation originates from their inherent parasitic parameters, which may be due to the junction or parasitic capacitances of the semiconductor.[1–5] Compared with these semiconductor switches, microelectromechanical system (MEMS) rf switches offer many benefits such as low insertion loss, good isolation, excellent linearity characteristics, and low power consumption.[6–15] In view of these aspects, many researchers have attempted to commercialize these MEMS switches for phase shifters, a variety of reconfigurable elements, and tunable filter applications.[16–19] Over the last decade, various types of micromechanical switches have been developed. Among these various types of switches, an electrostatically actuated rf switch and its package are proposed here. The basic concept design, fabrication, and experimentally measured results of these rf switches have been carried out in previous work.[20] This work focuses on the packaged switch design, performance simulations, and fabrication details. The proposed switch is a compound of a membrane and see-saw type of switch. Thick membranes are made of single crystalline bulk silicon to prevent "the membrane bending problem," which causes a gap change between the electrodes and the membrane. The increase of the driving voltage and its variation comes from this electrode and membrane gap change. This work also introduces a flexible spring that can operate at low voltages, and which has a pivot under the membrane for high restoring forces. When the membrane is actuated downward, it operates in a see-saw-like mode. This concept compensates for the high driving and restoring voltage characteristics of conventional see-saw mode actuated switches. A driving and restoring voltage decrease was also obtained, which was comparable to the membrane-type switch while maintaining high isolation similar to that of see-saw-type switches. MEMS switches consist of micrometer-sized membrane structures that are very easy to

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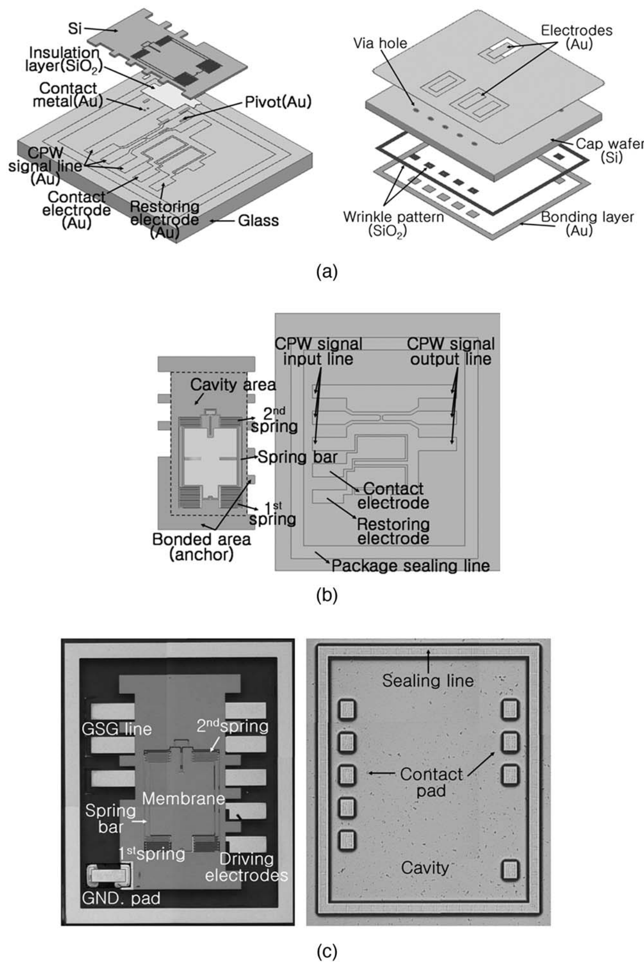

Fig. 1 The proposed rf switch and package cap wafer: (a) exploded image of the proposed rf switch and package cap wafer. (b) Top and backside view of fabricated rf switch. (c) Top and backside microscope image of the fabricated rf switch and package cap wafer.

break or damage, therefore they need to be hermetically sealed against various kinds of contamination sources.[21] To package the proposed rf switch, a cavity-etched silicon wafer is used as a cap wafer, and a sputtered Au layer with a thermocompressive bonding method is used as an intermediate bonding layer.

2 Design and Simulation

Figure 1 shows a 3-D and microscope image of the wafer-level packaged rf switch, with a bulk silicon membrane. On the glass wafer, a coplanar waveguide (CPW) line is designed and patterned for passing the rf signal as well as fabricating electrode pads for the operation of the membrane. The thick membrane with pivot has folded springs for the actuation that is formed via the silicon wafer. The signal line width of the CPW line is 150 μm and the gap between the signal and the ground line is 100 μm. Figure 1(b) shows the top and backside views of the fabricated rf switch. It can be seen that the end of the first folded spring is connected to the anchored silicon, which is bonded with glass. The end of the second folded spring is connected to the membrane, and the spring bar couples the first and second springs. A high resistivity silicon (HRS) wafer is used for the package cap wafer because it reduces the substrate loss of the rf signals. A cavity and hole for the signal line path to pass through is formed on the silicon wafer. A pure Au layer is used for the intermediate bonding layer, and the total size of the packaged switch is 1.2×1.5 mm. While the driving voltage is not applied to both electrodes, the switch is in the "off" state, and the initial gap between the signal and the ground line is 3 μm. When the dc driving voltage is applied to the contact electrode, the membrane is actuated downward and the contact pad metal connects the 20-μm gap of the broken CPW line. When the switch changes to the "on" state, the electrode and membrane maintained a 1-μm gap without bending or stiction because of the 30-μm-thick membrane and the pivot. This narrow gap also enables the switch to operate at a very low voltage. To change the switch to the "off" state, the dc voltage is applied to the restoring electrode and elevates the membrane. The pivot is used for the see-saw-mode operation, while the dc voltage is applied to the driving electrode or the restoring electrode.

To estimate the rf characteristic of the wafer-level package switch, a 3-D full-wave electromagnetic field simulator HFSS™, manufactured by Ansoft Company (Pittsburgh, Pennsylvania) has been used, and the simulated electromagnetic field distribution results of this design are shown in Fig. 2. The simulated insertion loss of this design is −0.15 dB at 2 GHz when the switch is in the "on" state, and the isolation is −33.6 dB when the switch is in the "off" state.

3 Experiment and Fabrication

3.1 *Device Fabrication*

The detailed fabrication process is shown in Fig. 3 in the form of a 3-D image of the switch. To minimize the coefficient of thermal expansion (CTE) mismatch problem, a 500-μm-thick Corning 7740 Pyrex glass wafer is used as a substrate,[22] and a 50/1000-nm Cr/Au is sputtered on the glass. This is defined by using photoresist, and is etched using a wet solution to fabricate the CPW line, the electrode, and the package sealing line. On the silicon wafer, a cavity form is patterned using a photoresist, and etched using a deep reactive ion etcher (DRIE). The silicon wafer used is a p-type (100) with a resistivity of 0.01 to 0.02 Ω·cm. A plasma enhanced chemical vapor deposition (PECVD) is used to deposit a 500-nm oxide insulation layer in the cavity, which is then patterned using a reactive ion etcher (RIE). A 50/450-nm-thick Cr/Au layer is deposited onto the insulation layer using a sputter, and is patterned by a wet etching method to fabricate the contact metal and the pivot. These two fabricated wafers are then dipped in $H_2SO_4 : H_2O_2 = 1:1$ solution and the 6:1 buffered oxide etcher (BOE) to clean the surface just prior to the bonding process, because minor contamination of the surface can significantly affect the bonding performance or strength.[23] The dipping time of these two solutions is 1 min and 10 sec. After the surface cleaning process, the Si and glass wafer are assembled using an anodic bonding method; the bonding temperature, pressure, and applied voltage are set to 370 °C, 100 N, and 550 V, respectively, and the duration time is set to 5 min. The silicon layer is ground and polished until only 30 μm remains after the bonding pro-

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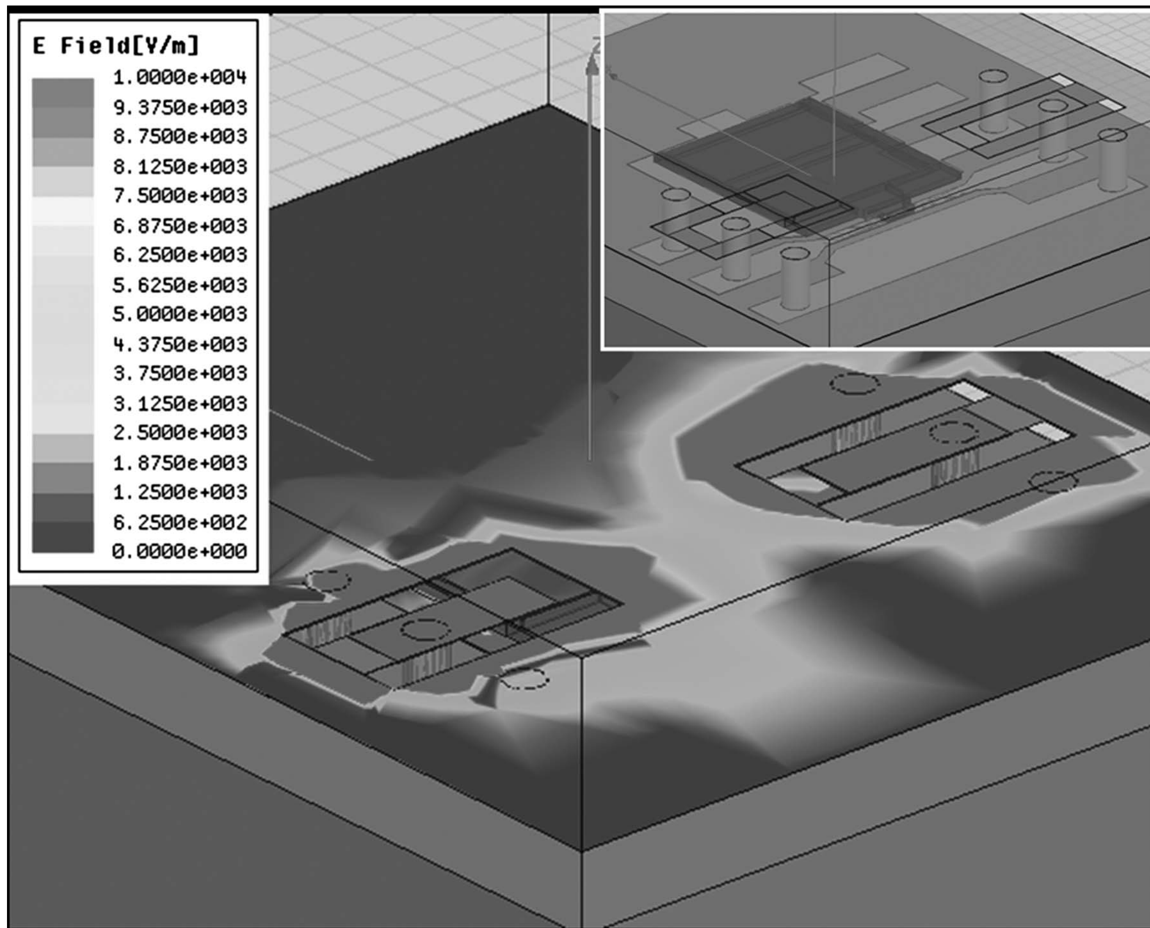

Fig. 2 Simulated electromagnetic field distribution results of the packaged rf switch.

cess is complete. The membrane structure, with springs and spring bars, is patterned at the rear side of the cavity etched pattern using a photoresist on the silicon layer, and is etched using a DRIE. The nonetched silicon pattern, which is bonded with the glass layer, becomes the anchor. The photoresist on the silicon is removed using a low temperature dry asher to prevent thermal stress and unwanted bending of structures.

3.2 *Cap Wafer Fabrication*

A cap wafer to package the switch uses an n-type high resistivity silicon (HRS) wafer, which has a resistivity of over 10 KΩ, to reduce the substrate loss of the rf signals. To make the package sealing line, which is composed of several fine pitch lines, a 1-μm-thick thermal oxide is grown by wet oxidation, and several fine pitch lines patterned using a GXR 601 photoresist. Wafers are dipped in the $H_2SO_4:H_2O_2=1:1$ solution to remove the photoresist after the oxide etching process. The width of the fabricated oxide line pattern is 5 μm, and the width of the etched oxide groove is 6 μm. A wrinkle shape pattern is clear in the cross section view of this sealing line, hence it is known as wrinkle shaped sealing line.

A Cr/Au 50/1000-nm thickness of the bonding layer, with a contact metal pad, is deposited using sputtering equipment, and the Cr/Au layer is patterned and etched using the wet etching method. After the etching process, the whole exposed silicon layer is etched by using DRIE to form the cavity, the sealing line, and the contact pad of the cap wafer simultaneously. A 50-μm depth of cavity is etched, and the size is 1915 × 1560 μm. The sealing line width is 50 μm and the contact pad size is 110 × 83 μm. The patterned photoresist is removed by acetone and a $H_2SO_4:H_2O_2=1:1$ solution. This cleaning is performed to remove not only any extra photoresist residue, but also any extra organic contaminants prior to the bonding process.

3.3 *Assembly of Device and Package Wafer*

The two wafers are aligned using the EV-620 aligner and placed into the SST international 3180 bonder. To prevent movement of the aligned wafers during the pumping or heating process, a 0.1-MPa initial pressure is applied. The bonding temperature, pressure, and duration time are set to 350 °C, 65 MPa, and 30 min, respectively. After the bonding process, the silicon cap wafer is ground and polished until the cap wafer is 150 μm thick. On the polished surface, a via-hole for the signal interconnection is patterned using an AZ 4330 photoresister and etched by the DRIE notch-free process. The shape of the via-hole is an elliptical design with dimensions of 80 and 50 μm. To form the interconnection metal line on the cap wafer and hole, a Cr/Au 50/2000 nm is sputtered and patterned. A photoresist spray

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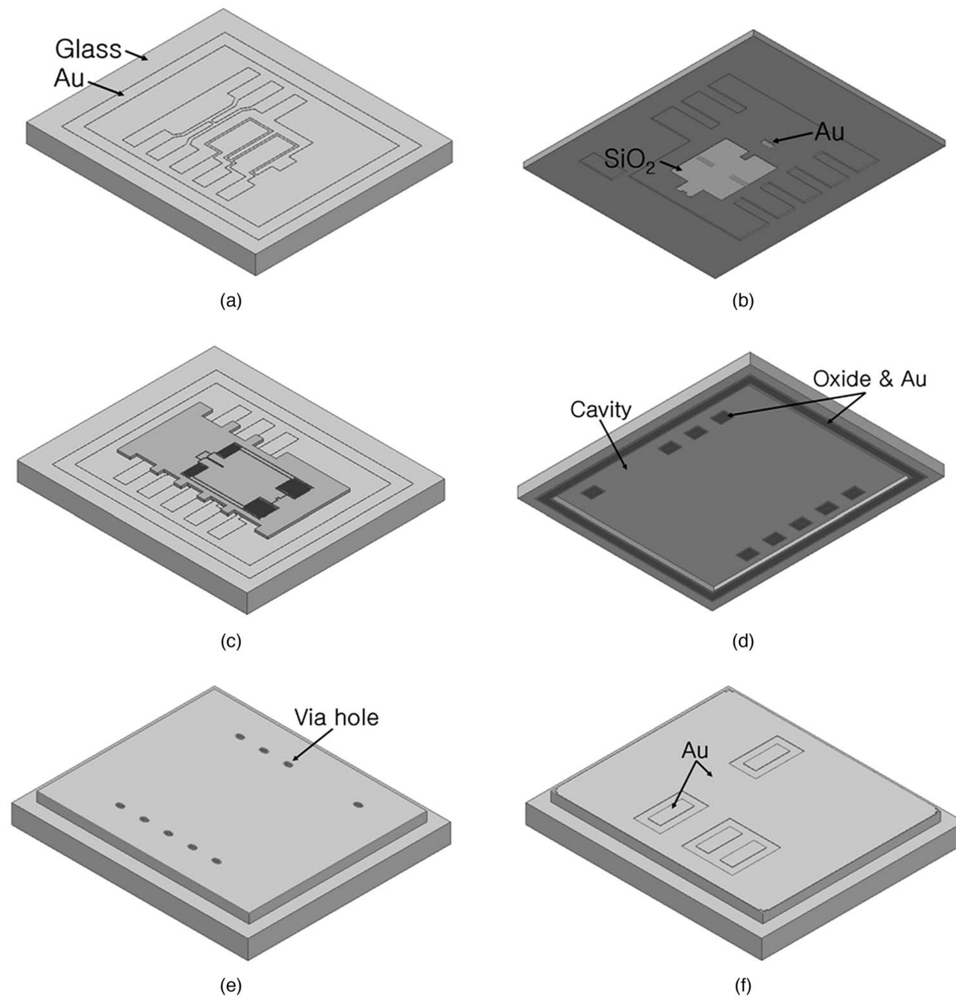

Fig. 3 The fabrication process for the packaged rf switch. (a) The signal line, electrodes, and sealing line are patterned on the glass wafer. (b) The insulation layer, pivot, and contact electrode are formed at the cavity of the silicon wafer. (c) The membrane structure and springs are formed by using a dry etcher after the glass and silicon bonding, and silicon polishing process. (d) The package sealing line and the interconnection pad are patterned at the silicon wafer. (e) The via-hole for the signal interconnection is patterned and etched using a deep dry etcher. (f) An Au metal line is deposited for signal line and via interconnection.

coater is used to overcome the coating failure due to the hole's sharp edge line, which cannot be coated when a normal spin coater is used; an exposed metal line can easily break down during the wet etching process. The Cr/Au layer is etched by using a wet etchant, and the photoresist is removed using the photoresist stripper. The full wafer-level packaged switches are shown in Fig. 4. After the package process, the package cap of the switch is decapsulated to ascertain the possibility for the permeation of water or any other solutions.

4 Results and Discussion

A thick-membrane-operated rf MEMS switch has been developed and packaged with a thermocompressive bonding method, using a sputtered thin Au layer. A thick membrane and pivot make it possible to maintain a very small gap between the electrodes and the membrane without bending, and low operation voltage can be achieved using a see-saw-mode operated design. A sacrificial layer is not used to fabricate the membrane structure, therefore the contamination and residue problems have been minimized during the

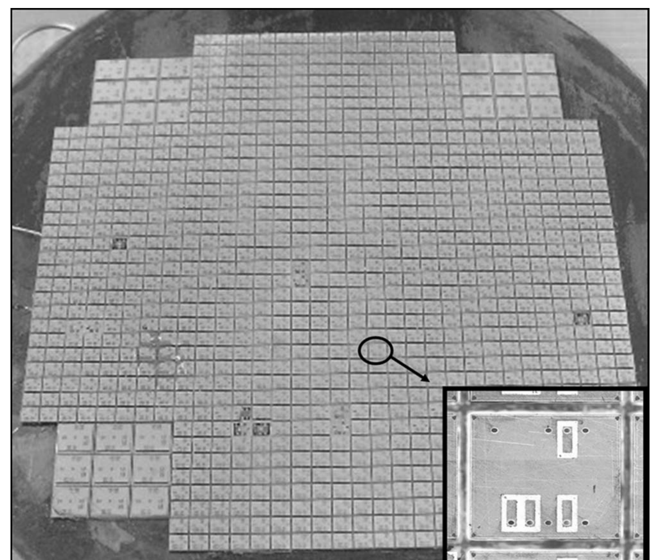

Fig. 4 Wafer-scale packaged rf switch.

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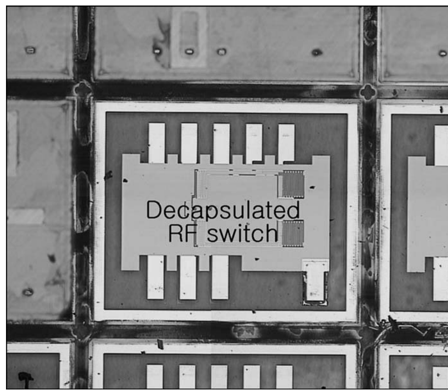

Fig. 5 The microscope image of the decapsulated switch.

removal of the sacrificial layer on the contact area. An HRS wafer has been used to package the rf switch, and a sputtered Au layer is used as an intermediate bonding material. After the package process has been completed, the package cap is decapsulated to ascertain permeation possibilities of any solution. As seen in Fig. 5, no watermark or residue solution can be found, and the rf characteristics of the packaged switch have been measured using a HP 8510C network analyzer with a 250-μm pitch size ground-signal-ground (G-S-G)-type Pico probe. Figure 6 shows the simulated and measured rf characteristics. The insertion loss of the packaged switch has been measured to be −0.43 dB, the isolation is −38.4 dB at 2 GHz, and the measured driving voltage is 16 V. It is presumed that the loss in the via-hole interconnection and switch contact caused the difference between the measured and simulated results. This packaged switch can be used for various applications such as a filter bank for 0.8 to 20-GHz applications, an antenna switching system, a phase shifter, or for reconfigurable systems.

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References

1. T. Seki, Y. Uno, K. Narise, T. Masuda, K. Inoue, S. Sato, M. Jojima, F. Sato, K. Imanaka, and S. Sugiyama, "Low-loss SPDT metal-to-metal contacts RF MEMS switch operated by electrostatic actuation," *Proc. SPIE* **6035**, 603506 (2005).
2. H. Mizutani and Y. Takayama, "A DC–60 GHz GaAs MMIC switch using novel distributed FET," *IEEE MTT-S Int. Microwave Symp. Tech. Dig.* **2**, 439–442 (1997).
3. H. A. C. Tilmans, W. D. Raedt, and E. Beyne, "MEMS for wireless communications: 'from RF-MEMS components to RF-MEMS-SiP'," *J. Micromech. Microeng.* **13**, S139–163 (2003).
4. G. M. Rebeiz, "RF MEMS switches: status of the technology," *Dig. 12th Int. Conf. on Solid State Sensors, Actuators, and Microsystems (Transducers'03)*, Boston, MA, June 8–12, 2003, Vol. **2**, pp. 1726–1729 (2003).
5. Z. Yao, S. Chen, S. Eshelman, D. Denniston, and C. Goldsmith, "Micromachined low loss microwave switches," *IEEE J. MEMS* **8**, 129–34 (1999).
6. J. N. Randall, C. Goldsmith, D. Denniston, and T. H. Lin, "Fabrication of micromechanical switches for routing radio frequency signals," *J. Vac. Sci. Technol. B* **14**, 3692–3696 (1996).
7. H. U. Rahman, J. Babaei, and R. Ramer, "RF MEMS switches: design and performance in wireless applications," *Proc. SPIE* **6800**, 680027 (2007).
8. N. S. Barker and G. M. Rebeiz, "Distributed MEMS true-time delay phase shifters and wideband switches," *IEEE Trans. Microwave Theory Tech.* **46**, 1881–1890 (1998).
9. Z. J. Yao, S. Chen, S. Eshelman, D. Denniston, and C. Goldsmith, "Micromachined low-loss microwave switches," *J. Microelectromech. Syst.* **8**(2), 129–134 (1999).
10. N. V. Lakamraju, B. Kim, and S. M. Phillips, "CMOS compatible RF MEMS switch," *Proc. SPIE* **5455**, 193–201 (2004).
11. J. B. Muldavin and G. M. Rebeiz, "High-isolation MEMS shunt switches, part 1: modeling," *IEEE Trans. Microwave Theory Tech.* **48**, 1045–1052 (2000).
12. S. P. Pacheco, L. P. B. Katehi, and C. T. C. Nguyen, "Design of low actuation voltage RF MEMS switch," *IEEE MTT-S Int. Microwave Symp. Dig.* **1**, 165–168 (2000).
13. B. A. Cetiner, H. Jafarkhani, Q. Jiang-Yuan, Y. H. Jae, A. Grau, and F. D. Flaviis, "Multifunctional reconfigurable MEMS integrated antennas for adaptive MIMO systems," *IEEE Commun. Mag.* **429**(12), 62–70 (2004).
14. C. W. Dyck, T. A. Plut, C. D. Nordquist, G. M. Kraus, G. D. Schmidt, K. L. Gass, P. S. Finnegan, I. C. Reines, and C. T. Sullivan, "Compact MMIC compatible RF MEMS switch," *Proc. SPIE* **4981**, 222–229 (2003).
15. C. W. Dyck, T. A. Plut, C. D. Nordquist, P. S. Finnegan, F. Austin, I. Reines, and C. Goldsmith, "Fabrication and characterization of ohmic contacting RF MEMS switches," *Proc. SPIE* **5344**, 79–88 (2004).
16. N. S. Barker and G. M. Rebeiz, "Optimization of distributed MEMS phase shifters," *IEEE MTT-S Int. Microwave Symp. Dig.* **1**, 299–302 (1999).
17. A. Ziaei, T. Dean, M. Charrier, P. Bondavalli, J. P. Polizzi, H. Legay, B. Pinte, E. Girard, and R. Gillard, "Design and fabrication of low loss RF MEMS switches for a broadband reflectarray," *Proc. SPIE* **5389**, 64–72 (2004).
18. M. Kim, J. B. Hacker, R. E. Mihailovich, and J. F. Denatale, "A monolithic MEMS switched dual path power amplifier," *IEEE Microw. Wirel. Compon. Lett.* **11**, 285–286 (2001).
19. D. Peroulis, S. Pacheco, and L. P. B. Katehi, "Tunable lumped components with applications to reconfigurable MEMS filters," *IEEE MTT-S Int. Microwave Symp. Dig.* **1**, 341–344 (2001).
20. J. S. Kim, S. W. Kwon, Y. T. Hong, H. M. Jung, S. H. Lee, C. H. Kim, K. S. Lee, B. K. Ju, and I. S. Song, "Variable pivot seesaw actuated RF MEMS switch for reconfigurable system application," *IEEE MEMS Dig.* **1**, 775–778 (2007).
21. H. W. Park, Y. K. Park, D. J. Lee, and B. K. Ju, "Packaging of the RF MEMS switch," *Proc. SPIE* **4593**, 234–243 (2001).
22. W. B. Choi, B. K. Ju, Y. H. Lee, M. R. Haskard, M. Y. Sung, and M. H. Oh, "Anodic bonding technique under low temperature and low voltage using evaporated glass," *J. Vac. Sci. Technol. B* **15**(2), 477–481 (1997).
23. G. Wallis and D. I. Pomerantz, "Field assisted glass metal sealing," *J. Appl. Phys.* **40**, 3946–3949 (1969).

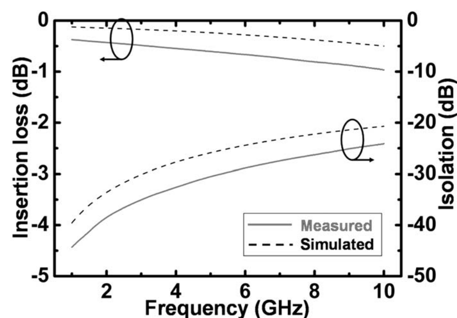

Fig. 6 rf characteristics of the simulated and measured rf switches.

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