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High-mobility pentacene thin-film phototransistor with poly-4-vinylphenol gate dielectric

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Abstract

An organic thin-film transistor was fabricated with pentacene as the active material and poly(4-vinyl phenol) as the gate-dielectric material. Atomic force microscope image shows that the pentacene film grows in the polycrystalline structure of the poly-4-vinylphenol (PVP) dielectric layer with the surface root-mean square (RMS) roughness of 6.0 nm and average grain size of 800 nm. The pentacene thin-film transistor exhibited a saturation field-effect mobility of 1.64 $cm^2/V\,s$, a threshold voltage of -18 V, a sub-threshold swing of 3.53 V/decade, on/off-current ratio of 7.1×10^4 and interface trap density of 5.39×10^{12} eV^{-1} cm^{-2}. The higher mobility of pentacene on poly(4-vinyl phenol) layer is attributed to the larger grain size of the pentacene.

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ABSTRACT

An organic thin-film transistor was fabricated with pentacene as the active material and poly(4-vinyl phenol) as the gate-dielectric material. Atomic force microscope image shows that the pentacene film grows in the polycrystalline structure of the poly-4-vinylphenol (PVP) dielectric layer with the surface root-mean square (RMS) roughness of 6.0 nm and average grain size of 800 nm. The pentacene thin-film transistor exhibited a saturation field-effect mobility of 1.64 cm^2/V s, a threshold voltage of −18 V, a sub-threshold swing of 3.53 V/decade, on/off-current ratio of 7.1×10^4 and interface trap density of 5.39×10^{12} eV^{-1} cm^{-2}. The higher mobility of pentacene on poly(4-vinyl phenol) layer is attributed to the larger grain size of the pentacene. The photoresponsive properties of the organic thin-film transistor were investigated under various illumination intensities. The photosensitivity was measured as 1.46 at an illumination intensity of 100 mW/cm^2 at the off state. This suggests that the pentacene thin-film transistor shows a phototransistor behavior.

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1. Introduction

Organic thin-film transistors (OTFTs) have been developed for applications in low-cost electronic circuits, large-area displays, sensors, etc., in recent years [1–4]. Organic semiconductors based on organic compounds and polymers are the most interesting candidate materials for OTFTs due to their low fabrication cost and flexibility. Although organic semiconductors have low mobility, the studies made on performances of OTFTs suggest that they can be competitive for existing as novel OTFT applications [5]. The advantage of the field-effect transistor (FET) technique in investigating organic conducting materials is that the amount of the carrier can be regulated by the gate voltage without chemical doping [6]. The performance of OTFTs has been significantly improved using organic dielectric materials. The one of the transistor performances is lower power consumption that is related to lower operating voltage for practical applications. The other is higher device speed that has to do with higher carrier mobility [7]. How to improve the performance of devices is still important problem for the researchers in the field of organic electronics [8]. It is evaluated that the perfor-

mance of the OTFT can be improved using novel organic insulator layer. Thin-film transistors based on pentacene are usually fabricated by using bottom gate TFT structures, in which, the pentacene film is prepared on top of a dielectric. The performance of the pentacene TFTs strongly depends on the properties of the dielectric, the growth conditions of the pentacene molecules and the structural properties of the film [9].

In this paper, we have evaluated that use of PVP as gate insulator may improve the mobility of the pentacene OTFT. Additionally, we have investigated the current–voltage characteristics and photoresponsive properties of a pentacene OTFT.

2. Experimental

Organic thin-film transistor was fabricated with the widely used bottom-gate and top contact geometry as shown in Fig. 1. 100-nm-thick indium tin oxide (ITO, sheet resistance ~10.0 ohm/sq) layer was deposited on a glass substrate by the sputtering evaporation. Next, a 240-nm-thick cross-linked PVP film served as a gate dielectric layer. To prepare a poly-4-vinylphenol (PVP) solution, the PVP powder (Sigma–Aldrich, Mw < 20,000) was mixed with 8 wt% of propylene glycol monomethyl ether acetate (PGMEA) and then we added the cross-linking agent, poly(melamine-co-formaldehyde) (Sigma–Aldrich, Mw < 511), to the PVP solution with a ratio of 1:20. To form a PVP dielectric film, the PVP solution was coated on the glass substrate with an ITO electrode and a curing process
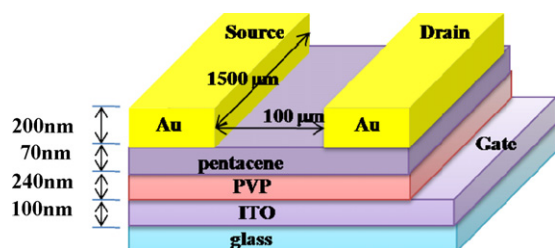
Fig. 1. Schematic structure of OTFT.

was conducted at 200 °C for 10 min on a hot plate to enforce the cross-linking of the PVP polymer. Subsequently, a 70 nm thick pentacene (Sigma–Aldrich, ~99% purity) active layer was deposited on the PVP dielectric layer with a deposition rate of 0.4 Å/s under a base pressure of 1×10^{-6} Torr by a thermal evaporator (DOV Co., Ltd.). Finally, the 200 nm thick Au source and drain electrodes were deposited through a shadow mask by the thermal evaporator. The channel width and length of the transistor were 1500 and 100 μm, respectively. The surface morphology of the pentacene film on PVP layer was analyzed by atomic force microscopy (AFM, Veeco, Dimension 3100). The transistor characteristics of the transistor were measured by using a semiconductor characterization system (Keithley SCS 4200) in a dark box. The photosensitive properties of the transistor were performed using a monochromatic halogen lamp of 200 W.

To further investigate the molecular ordering in pentacene film, we used X-ray diffraction (XRD, D/max 2200 V) spectroscopy in a symmetric reflection coupled θ–2θ arrangement with a *Cu Ka$_1$* radiation ($\alpha\lambda_{K\alpha1}$ = 1.54 Å) X-ray source.

3. Results and discussion

Fig. 2 shows the AFM image of the pentacene on PVP layer. As seen in the image, the pentacene film grows in the polycrystalline structure of the PVP dielectric layer. The surface root-mean square (RMS) roughness and average grain size for the pentacene film were found to be 6.0 and ~800 nm, respectively. These parameters have an important effect on the performance of the OTFTs. The mobility is affected by these parameters, because the mobility is very sensitive to the degree of molecular ordering of the pentacene film. The grain
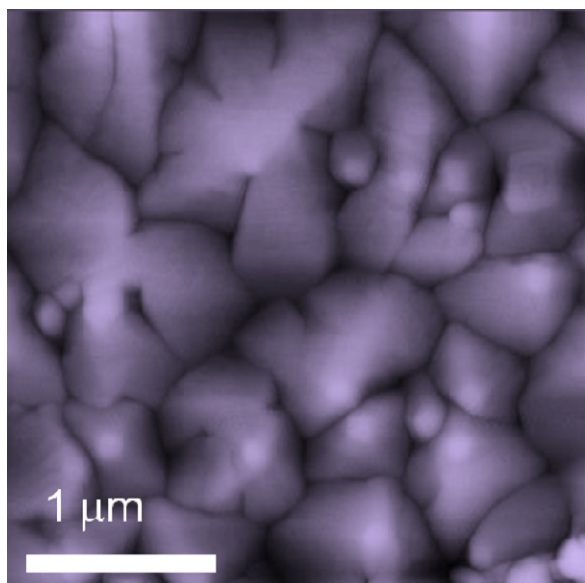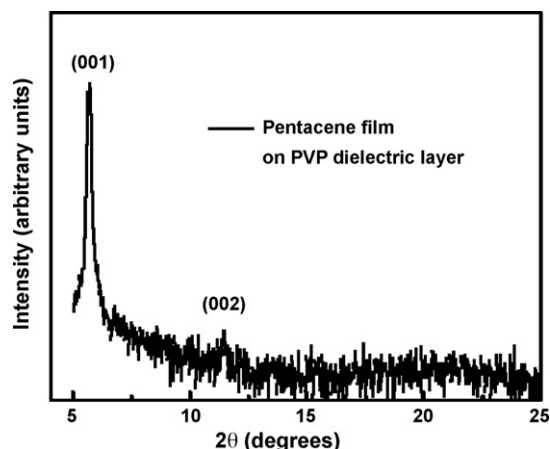

Fig. 3. An XRD spectroscopy result of pentacene film with an average thickness 70 nm deposited on a PVP/ITO/glass substrate.

size of the pentacene film on PVP layer changes the mobility, i.e., the larger grain size of the pentacene gives the higher mobility. This is attributed to the π-electron orbitals overlap between neighboring pentacene molecules [10].

Fig. 3 shows XRD results for an 70-nm-thick pentacene thin film grown on polymer PVP insulator. The XRD result showed good molecular ordering for vaccum deposited thin film and the same diffraction peaks as bulk crystal pentacene [11,12]. Also, a strong sharp peak observed at 5.7° as shown in Fig. 3, indicated a well-organized molecular structure.

Fig. 4 is a topographic image of the PVP surface on a ITO-deposited glass substrate showing a very smooth surface with RMS roughness of 0.347 nm. We saw that the surface film was without any surface height difference. If the dielectric film has poor surface roughness, then this roughness leads to valleys in the channel region. These valleys may act as carrier traps with a number of scatterings.

Fig. 5 shows output characteristics of the pentacene OTFT. For the operating of transistor, the two Au contacts are designated as the drain and source, respectively and gate voltage is applied to the ITO glass substrate. In this case, the drain-to-source current then flows between the Au contacts via pentacene organic semiconductor. The drain-source current is controlled by gate voltage. Fig. 5 shows the current–voltage characteristics of the OTFT under various gate voltages. As seen in Fig. 5, the current (I_{ds}) almost increases linearly with V_{ds} at negative gate voltage. This suggests that this device is a voltage-controlled resistor regulated by the gate voltage. The increment of drain-source current increases with gate voltage. This suggests that positive carriers are generated in the active pentacene organic semiconductor layer on the application of negative gate voltage. The OTFT device works under accumulation mode and shows *p*-channel characteristics. The output characteristics of the transistor indicate a saturation region at negative V_G voltages. The drain-source current for the OTFT transistor is expressed for linear
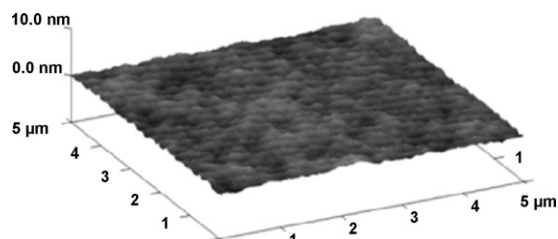

Fig. 2. AFM image of the pentacene on PVP layer.

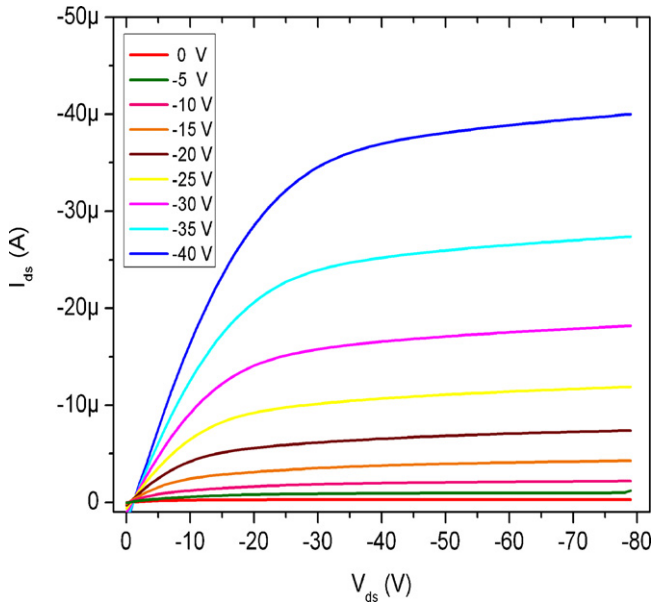Fig. 4. AFM images of the PVP film on ITO glass substrate.

Fig. 5. Output characteristics of the transistor at various V_g voltages.

and saturation regions [13–15],

$$I_{ds} = \frac{W}{L}\mu C_i \left[(V_g - V_{th})V_d - \frac{V_d^2}{2} \right] \quad \text{for linear region} \quad (1)$$

and

$$I_{ds} = \frac{W}{2L}\mu C_i (V_G - V_{th})^2 \quad \text{for saturation region} \quad (2)$$

where I_{ds} is the drain-source current, W is the width of channel, L is the channel length, C_i is the capacitance per unit area of the insulator (C_i of PVP insulator with 240 nm thick is 14.8 nF/cm^2). V_g is the gate voltage, μ is the mobility and V_{th} is the threshold voltage. The drain current increases with V_{ds} and then starts to saturate. This is indicating of ohmic pentacene/Au contacts. The ideal behavior is when $V_d = 0$ V, $I_d = 0$ A. In contrast, significant I_D offset is common in OTFTs [15,16]. The transistor shows an ideal I–V behavior with the PVP gate dielectric layer.

Fig. 6 shows the current–voltage characteristics of I_{ds}–V_g under −80 V. The ratio of on-current/off-current (I_{on}/I_{off}) for the transistor
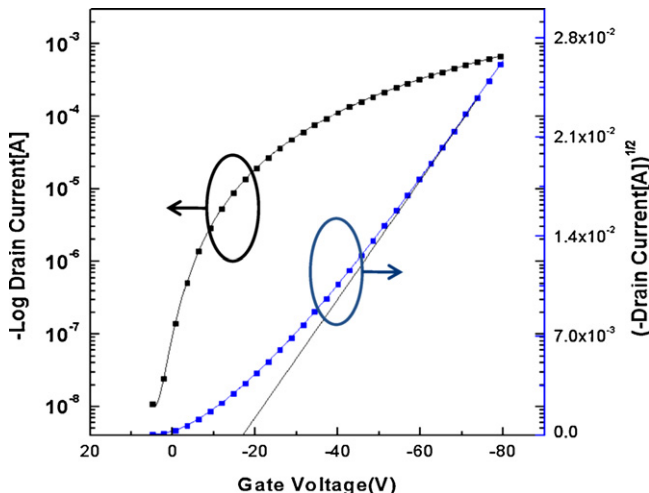

Fig. 6. Plots of $\log I_{ds}$–V_g and $I_{ds}^{1/2}$–V_g of the transistor under −80 V.

was found to be 7.1×10^4. The threshold voltage was determined from the plot of square root of the drain current versus gate voltage ($I_{ds}^{1/2}$–V_g) as shown in Fig. 6 and was found to be −18 V. The V_{th} can change due to trap states at the interface. These charges initially are trapped at the interface and then, these charges can participate to the drain current upon applying a gate voltage.

The mobility μ was estimated using the following relation:

$$\mu = \frac{2L}{WC_i} \left(\frac{dI_{ds}^{1/2}}{dV_g} \right)^2 \quad (3)$$

The mobility of the OTFT was determined from the plot of $I_{ds}^{1/2}$–V_g and was found to be 1.64 cm^2/V s. The obtained mobility (1.64 cm^2/V s) value of the pentacene of 70 nm transistor with PVP dielectric gate layer of 240 nm is higher than that of mobility (0.15 cm^2/V s) of pentacene of 100 nm with PVP gate layer of 922 nm [17] and mobility (0.10 cm^2/V s) of the pentacene of 100 nm with PVP gate layer of 300 nm thin-film transistors [18]. We have evaluated that the increase in the mobility is due to the thickness of the PVP layer. It is well known that in a FET, the gate voltage switches the transistor with insulator thickness and dielectric constant. Thus, for a FET, high dielectric constant and low thickness is desired and the mobility in OTFT strongly depends on the surface roughness of the organic layer and dramatically decreases with increased roughness. The higher mobility is resulted from the larger grain size and lower roughness. It is shown that a pentacene film with a larger grain size yields higher carrier mobility in literature [19,20]. Also, it is evaluated that the higher mobility reported for pentacene layer could be due to a higher conductivity of crystalline phase forming domains extending from source to the drain as in a network of parallel resistances (dominated by the most conductive ones).

The sub-threshold swing SS for the transistor was determined from the plot of $\log I_{ds}$ versus $\log V_g$ and was found to be 3.53 V/decade. This value of the transistor controls the voltage swing that is required to turn a transistor from "off" to "on" state. The sub-threshold behavior of the drain current is attributed to the distribution of defect states in the band gap. Thus, the maximum number of present interface traps can be calculated by the following relation [21],

$$D_{it} = \left[\frac{S \, \log(e)}{kT/q} - 1 \right] \frac{C_i}{q} \quad (4)$$

where k is the Boltzmann constant, T is the temperature and q is the electronic charge. The D_{it} value for the transistor was found to be 5.39×10^{12} eV^{-1} cm^{-2} and this value is lower than that of the D_{it} value (4.04×10^{13} eV^{-1} cm^{-2}) of pentacene of 100 nm with PVP gate layer of 300 nm thin-film transistor [22]. The lower trap intensity of the transistor causes the lower sub-threshold swing.

The drain-current curves of the pentacene thin-film transistor under various illumination intensities from 100 to 20 mW/cm^2 are shown in Fig. 7. The generation of charge carriers starts when light with photon energy is equal or higher than bandgap energy is absorbed and in turn, the drain-source current of the transistor increases. This indicates that light can play a role as an additional terminal that optically controls device operation with conventional third terminals, source, drain, and gate electrodes [23]. The drain current of the transistor increases with increasing illumination intensity. This suggests that the pentacene thin-film transistor shows phototransistor behavior. The photosensitivity ($R = I_{ph}/I_{dark}$) was measured as 1.46 at an illumination intensity of 100 mW/cm^2 under $V_g = 0$. The photosensitivity of the transistor studied is almost the same with the pentacene thin-film transistor fabricated on n-Si substrate with thermally oxidized SiO$_2$ as a gate insulator [24]. This value is low. Liu et al. [25], have found that the photosensitivity of polymer thin-film
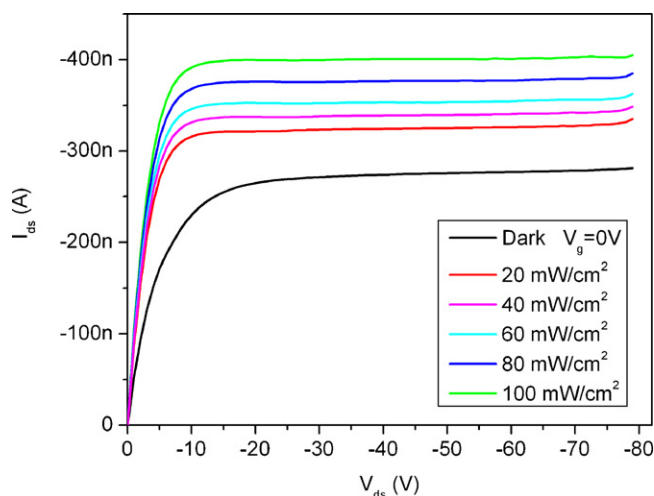
Fig. 7. Output characteristics of the transistor at various illumination conditions.
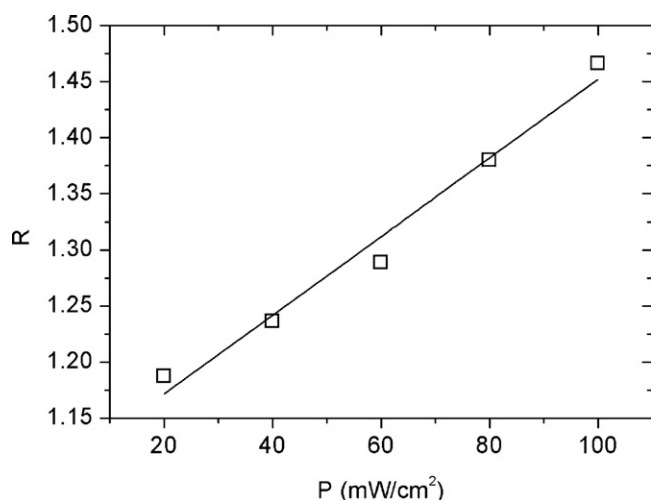

Fig. 8. Plot of R versus P of the transistor.

transistors based on poly(2-methoxy-5-(2′-ethyl-hexyloxy)-1,4-phenylenevinylene) depends on the gate voltage. In the study made by Liu et al., when using the above-threshold mode, the on-state current increased slightly under illumination and the photosensitivity (I_{ph}/I_{dark}) is 1.93 at an illumination intensity of 1200 lux and a gate voltage of −25 V. However, for the sub-threshold mode, the off-state current significantly increases with illumination intensity and the maximum photosensitivity is 198 ± 17 at the same illumination intensity and a gate voltage of −5 V [25]. These results indicate that the photocurrent of an OTFT is modulated by the gate voltage [24]. Another measure, which is related to the photosensitivity, is the ratio of total drain current under illumination to drain current in the dark, which is referred to as the photoresponse. In the off-state, the photogenerated charge carriers are the major contribution to the free carrier density in the channel, and are strongly dependent on the incident irradiance.

The photoresponse R dependence of illumination for the transistor can be analyzed by the following relation [26]:

$$R = AP^{\gamma} \tag{5}$$

where A is a constant and P is the illumination intensity and γ is a constant. Fig. 8 shows the plot of R versus P for the transistor. The γ values for 0.5 and 1.0 correspond to bimolecular recombination and monomolecular recombination mechanism, respectively [27].

Whereas, the value of the exponent lies between 0.5 and 1.0 for continuous distribution of trapping centers [28]. The response values of the transistor increases linearly with the illumination intensity. The γ value for the transistor was found to be 0.12. The $\gamma = 0.12$ value for the pentacene phototransistor indicates the participation of another recombination path.

4. Conclusions

We have studied the electrical characteristics of organic field-effect transistor fabricated with pentacene as the active material and poly(4-vinyl phenol), as the gate material. The pentacene OTFT shows a saturation field-effect mobility of 1.64 cm^2/V s. The higher mobility of pentacene on poly-4-vinylphenol layer is attributed to PVP dielectric layer and the larger grain size of the pentacene. The transistor prepared behaves as a photoresponsive organic field-effect transistor.

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