Organic Thin Film Transistor with Poly(4-vinylbiphenyl) Blended 6,13-Bis(trisopropylsilylethylene)pentacene on Propylene Glycol Monomethyletheracetate Dielectric Surface

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Abstract:

This paper presents the latest results in the use of soluble materials, such as organic semiconductors (OSC) and gate-dielectrics, for simplified processing of organic thin film transistors (OTFTs). In this work, the fabrication of a solution-processed OTFT, with 6,13-bis(trisopropylsilylethylene)pentacene (TIPS-pentacene) and TIPS-pentacene mixed with poly(4-vinylbiphenyl) (PVBP) as the OSC, and propylene glycol monomethyletheracetate (PGMEA) as the gate-dielectric, is described. From electrical measurements, we observed exemplary $I-V$ characteristics for these TFTs. Device performance characteristics have been obtained, including the charge carrier mobility ($\mu$) of $1.47 \times 10^{-2}$ cm$^2$/Vs, threshold voltage ($V_T$) of $-11.36$ V, current on/off ratio ($I_{on}/I_{off}$) of $1.08 \times 10^{6}$, sub-threshold swing (SS) of $2.13$ V/decade for an OTFT with PVBP blended TIPS-pentacene and $\mu$ of $1.39 \times 10^{-4}$ cm$^2$/Vs, $V_T$ of $0.7$ V, $I_{on}/I_{off}$ of $1.64 \times 10^{5}$, SS of $4.21$ V/decade for an OTFT without polymer binder, individually.
Organic Thin Film Transistor with Poly(4-vinylbiphenyl) Blended 6,13-Bis(triisopropylsilylthynyl)pentacene on Propyleneglycolmonomethyletheracetate Dielectric Surface

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This paper presents the latest results in the use of soluble materials, such as organic semiconductors (OSCs) and gate-dielectrics, for simplified processing of organic thin film transistors (OTFTs). In this work, the fabrication of a solution-processed OTFT, with 6,13-bis(triisopropylsilylthynyl)pentacene (TIPS-pentacene) and TIPS-pentacene mixed with poly(4-vinylbiphenyl) (PVBP) as the OSC, and propyleneglycolmonomethyletheracetate (PGMEA) as the gate-dielectric, is described. From electrical measurements, we observed exemplary I–V characteristics for these TFTs. Device performance characteristics have been obtained, including the charge carrier mobility (μ) of 1.47 × 10⁻² cm²/Vs, threshold voltage (Vₜ) of −11.36 V, current on/off ratio (Iₚ/Iₚ₀) of 1.08 × 10⁴, sub-threshold swing (SS) of 2.13 V/decade for an OTFT with PVBP blended TIPS-pentacene and μ of 1.39 × 10⁻⁴ cm²/Vs, Vₜ of 0.7 V, Iₚ/Iₚ₀ of 1.64 × 10³, SS of 4.21 V/decade for an OTFT without polymer binder, individually.

Keywords: 6,13-Bis(triisopropylsilylthynyl)pentacene, Propyleneglycolmonomethyletheracetate, Organic Thin Film Transistor.

1. INTRODUCTION

Solution-processed organic semiconductors (OSCs) and gate-dielectrics are of interest because they allow the fabrication of flexible electronic devices using low-cost manufacturing approaches, such as spin-coating,¹ drop-casting,² screen printing,³ spray printing,⁴ and roll-to-roll processing.⁵

Recently, several promising solution-processable OSCs, namely 6,13-bis(triisopropylsilylthynyl)pentacene (TIPS-pentacene) have been identified; their electrical properties, measured from the field effect mobilities and current on/off ratios of the resulting organic thin film transistors (OTFTs), often rival those of thermally evaporated pentacene. Also, solution-processed gate insulators are important as they can provide an inexpensive fabrication approach. Therefore, many groups have studied not only solution-processable OSCs, but also solution-processable gate insulators such as poly(4-vinylphenol (PVP),² siloxane-based spin-on glass (SOG),⁶ polypivalcohol (PVA),⁷ poly(methyl-methacrylate) (PMMA)⁸ and poly(vinyl-cinnamate) (PVCN)⁹ for optimizing the device characteristics.

The electrical characteristics of OTFTs depend on the interface states between the OSC and the gate insulator. The molecular ordering of the smooth gate insulator is one of the determining factors for obtaining large carrier mobilities in OTFTs because the carrier transportation strongly depends on the overlap between the neighboring grains and the molecules. The gate insulator with only a slight surface roughness is one of the key factors for realizing the device optimization. This work reports the results of an investigation of solution-processed OTFTs, using polymer binder blended semiconductor; TIPS-pentacene mixed with poly(4-vinylbiphenyl) (PVBP) as the OSC and...
propyleneglycolmonomethyletheracetate (PGMEA) with a very smooth surface, as the gate-dielectric. Especially, we compare the performance of devices using TIPS-pentacene with and without polymer binder in order to confirm the effects of the polymer binder mixture.

2. EXPERIMENTAL DETAILS

The device configurations used in this work are shown in Figure 1(a), where a bottom gate and bottom contact structure has been used to characterize the OTFT. The devices were processed on a pre-cleaned, heavily doped, n-type silicon wafer acting as the gate electrode. The gate insulator, PGMEA (ZWD6216-6, Zeon Co. Ltd.), was spin-coated on an HF-treated silicon surface at a spin rate of 7,000 rpm for 10 s, and baked at 100 °C for 90 s using a hotplate in air. Gold source/drain electrodes were deposited by an electro-beam evaporator and a shadow mask was also used to define the source and drain electrodes. The channel width (W) and length (L) were 500 μm and 20 μm, respectively. Next, TIPS-pentacene (used as synthesized, Fig. 1(c))10 mixed with PVBP (Sigma-Aldrich, used as received, Figs. 1(b and d)) film was deposited by drop-casting and finally, the coated TIPS-pentacene-based device was annealed using a hotplate at 110 °C for 60 s. After the device fabrication, a Keithley SCS/4200 semiconductor characterization system was used to probe the devices in air ambient at room temperature and in dark condition.

To observe the topographical features of the samples, a field-emission scanning electron microscope (FE-SEM, Hitachi S-4300) and an atomic force microscope (AFM, XE-100 system, PSIA Inc.) were used.

Fig. 1. (a) Bottom contact device geometry used to characterize the device prepared by spin-coating PGMEA as the gate dielectric and drop-casting TIPS-pentacene mixed with/without PVBP as the OSC. (b) Chemical structure of poly(4-vinylbiphenyl). (c) photo-images of TIPS-pentacene powder and (d) polymer binder of PVBP.

Fig. 2. AFM images of drop-casted TIPS-pentacene films on glass substrate. (a) 2D and (b) 3D plots for surface morphologies of TIPS-pentacene without PVBP (RMS roughness: 303.99 nm, scan size: 10 μm × 10 μm). (c) 2D and (d) 3D plots for surface morphologies of TIPS-pentacene with PVBP (RMS roughness: 35.54 nm, scan size: 10 μm × 10 μm).
3. RESULTS AND DISCUSSION

For the gate insulation layer in the proposed device, PGMEA (dielectric constant = 3.44), is mostly used as an insulator material for low molecular electro-luminescence (EL) and polymer EL with alkaline development processing.11 PGMEA with high resistance and wide development latitudes can be made to a round pattern profile around the corner of the bank by only baking after fabrication of the insulating bank formation on a substrate via photo-lithography.

To confirm surface morphologies of OSCs such as TIPS-pentacene with and without PVBP, we investigated AFM images of the drop-casted OSC films on a glass substrate. Figure 2 shows the AFM images of the TIPS-pentacene without and with polymer binder, as shown in Figures 2(a)–(d), respectively, and the bright areas in the images have been interpreted as regions of increased film thickness. Here, Figures 2(a and c) are the 2-dimensional (2D) AFM images and Figures 2(b and d) are the 3D AFM images. The root mean square (RMS) roughness values of the TIPS-pentacene film with PVBP and TIPS-pentacene film are 35.54 nm and 303.99 nm, over 10 × 10 μm² area, respectively. The drop-casted TIPS-pentacene film without polymer binder shows a non-uniform coverage over the glass substrate as shown in Figures 2(a–b), but more uniform coverage over the glass substrate can be seen at TIPS-pentacene film with polymer binder as shown in Figures 2(c–d). Also, the grain size of the TIPS-pentacene layer mixed with PVBP is generally larger than TIPS-pentacene layer without polymer binder as shown in Figures 2(a–d). The grain size of OSCs in OTFTs can affect the mobility considerably due to a number of grain boundaries that may act as the carrier trap sites.6 Generally, having more grain boundaries leads to more potential barriers, which in turn limits the distance that a charge can move without running into an obstacle; thus a larger grain size is advantageous for the movement of the charges.12

Figure 3(a) shows a cross-sectional FE-SEM image of the PGMEA film on the silicon wafer layer and it reveals a void-free, defect free, and well covered uniform film. The thickness of the gate insulator is 380 nm, as shown in Figure 3(a). Figure 3(b) shows a tilted view FE-SEM image of the drop-casted TIPS-pentacene on the pre-deposited PGMEA layer. This surface morphology has many knoll-like shapes, and the thickness of the OSC is about 800 nm. In addition, Park et al. reported that TIPS-pentacene film, formed by drop-casting, has the best molecular order when compared with that of spin- and dip-casting methods. Thus,

![Fig. 3](image_url)  
(a) Cross-sectional FE-SEM images of the spin-coated PGMEA film on silicon substrate. (b) FE-SEM (with an apparent viewing angle of 8°) for drop-casted TIPS-pentacene film on the PGMEA film.

![Fig. 4](image_url)  
AFM images of the (a) PGMEA film spin-coated at 7,000 rpm and (b) TIPS-pentacene film drop-casted from a 2 wt% monochlorobenzene solution (scan size: 1 μm × 1 μm).
drop-casted TIPS-pentacene based OTFT exhibits better device performance than other casting methods and therefore the OSC film was deposited by drop-casting.

Figures 4(a) and (b) show the AFM images of PGMEA and TIPS-pentacene mixed with polymer binder films, respectively. Here, this binder mixed with the TIPS-pentacene acts as an adhesion layer, as well as a non-polar capping layer, to overcome the problem of poor compatibility between the TIPS-pentacene and the gate dielectric layer at their interface.

It is apparent that an extremely smooth surface is favorable for achieving good performance, since the surface roughness of the gate dielectric film is a primary factor in obtaining high carrier mobility. Figure 4(a) is a topographical image of the PGMEA surface that shows a very smooth surface with RMS roughness of 0.12 nm over 1 × 1 μm² area. It was clearly seen that the surface film had negligible surface height differences. If the dielectric film has poor surface roughness, this leads to forming valleys between the gate dielectric and the gate electrode. These valleys can act as carrier traps with a number of scatterings so OTFTs that have a low surface roughness film exhibit good electronic performances. Also, it has already been confirmed that the surface roughness of PGMEA is smoother than that of thermally grown SiO₂ with an RMS roughness of 1.08 nm.

Figure 4(b) is an AFM image of TIPS-pentacene film that has an RMS roughness of 42.19 nm over 1 × 1 μm², which has been recorded by scanning the local area along Figure 3(b). It was clearly seen that the surface film showed round hill-like surfaces without any preferential orientation.

Figure 5 shows the electrical characteristics of OTFT using the drop-casted TIPS-pentacene as an active channel layer and the spun-on PGMEA as a gate dielectric layer on the Si wafer. Figure 5(a) shows the drain current (I_D) and drain voltage (V_D) characteristics. The presence of large drain current offset in a low gate bias is due to the leakage current in the output curve because of a poor film forming property in TIPS-pentacene only. The
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Table 1. OTFT parameters (field effect mobility (µ) threshold voltage (Vt), current on/off ratio (ION/OFF), and sub-threshold slope (SS)) extracted from the transfer curves of OTFTs with and without (w/o) PVBP.

<table>
<thead>
<tr>
<th>Devices</th>
<th>µ [cm²/Vs]</th>
<th>Vt [V]</th>
<th>ION/OFF</th>
<th>SS [V/decade]</th>
</tr>
</thead>
<tbody>
<tr>
<td>OTFT w/o PVBP</td>
<td>1.39 × 10⁻⁴</td>
<td>0.7</td>
<td>1.64 × 10⁴</td>
<td>4.21</td>
</tr>
<tr>
<td>OTFT with PVBP</td>
<td>1.47 × 10⁻²</td>
<td>-11.3</td>
<td>1.08 × 10⁴</td>
<td>2.13</td>
</tr>
</tbody>
</table>

poor interfacial contact between the active layer and the dielectric layer can be expected. Also, we had observed this similar phenomenon through the OTFTs using standard TIPS-pentacene without the polymer binder on a thermally grown SiO2/Si wafer.14 Figure 5(b) shows the transfer characteristics of OTFT using TIPS-pentacene without the polymer binder. The gate leakage current is increased as the gate voltage (Vg) is increased, shown in Figure 5(b). This appearance may have been caused by the poor film properties. From the electrical output and transfer curve, shown in Figure 5, TIPS-pentacene/PGMEA-based OTFT had and extracted mobility (µ) of up to 1.39 × 10⁻⁴ cm²/Vs, threshold voltage (Vt) of 0.7 V, current on/off ratio (ION/OFF) of 1.64 × 10⁴, and sub-threshold swing (SS) of 4.21 V/decade.

Figures 6(a) and (b) show the output and transfer curves, respectively, for an OTFT with TIPS-pentacene mixed with PBVP and PGMEA insulator. The output characteristics for several gate voltage values are shown in Figure 6(a), where the Id saturates. The responses for Vg are much lower than that of the Vt (i.e., the linear region of a well behaved transistor) and show highly linear behavior, which is consistent with the ohmic contacts between the semiconductor and the gold electrodes. Also, the Id–Vg characteristics exhibited pinch off and showed typical p-type OTFT working in an accumulation mode.

Figure 6(b) shows transfer characteristics which were taken in 1 V gate steps from +10 V down to -80 V with a delay of 0.3 s between the steps. The saturation regime (Vg = -40 V) mobility was calculated based on the following standard TFT equation: ID = (WC/L2)µ(VG-VT)², where the insulator capacitance per unit area, C = 8.01 × 10⁻⁹ Fcm⁻², W = 500 μm, and L = 20 μm. The Vg was determined from a linear plot of the square root of the drain current (Vd/Vg) extrapolated to the x-axis intercept. For this device, parameters were obtained such as µ and the Vt, which were found to be 1.47 × 10⁻² cm²/Vs and -11.36 V, respectively. The SS defined as the voltage required to increase the ID by a factor of 10, is given by SS = dVg/d(log>ID) and therefore from the straight line (Log(ID) vs. Vg) in Figure 6(b), the ION/OFF and SS are 1.08 × 10⁴ and 2.13 V/decade, respectively. Additionally, the gate leakage current of the proposed device is below 3.5 nA at maximum Vg, as shown in Figure 6(b). Such parameters for all our devices are summarized in Table I.

4. CONCLUSION

The solution-processed OTFT has been fabricated based on TIPS-pentacene and PGMEA. Especially for PGMEA, photo-patternable gate dielectrics with very smooth surface roughness have been used, since photo-patterning of the gate dielectric layer is one of the important issues for display applications because it simplifies the process of manufacturing TFT arrays. Although the gate insulator layer was fabricated by the spin-coating method in the total area of substrate (i.e., not the patterned gate insulator), it has been confirmed in this work that PGMEA gate dielectrics can be applied to make OTFTs. Therefore, the PGMEA could be forecasted to be a promising candidate among a variety of organic gate dielectric materials for solution-processed electronic devices.

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