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Scaling down of amorphous indium gallium zinc oxide thin film transistors on the polyethersulfone substrate employing the protection layer of parylene-C for the large-scale integration

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KEYWORDS and PACS

Keywords

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Amorphous oxide semiconductors have been attracted with many advantages, such as room-temperature process availability, good-uniformity, high transparency in visible region (400–700 nm), and high mobility. The amorphous indium gallium zinc oxide (a-IGZO), one of most attractive materials, has been investigated by many researchers.[1–4] High mobility of a-IGZO is originated from the larger *ns*-orbital of the metal cation than 2*p*-orbital of oxygen anion.[1] Recently, a-IGZO has been applied as an active layer of thin film transistors (TFTs). Also, polyethersulfone (PES) substrate is widely used to flexible devices as a substrate. However, in general, PES substrate could be damaged by acids and solvents. As a matter of fabricating the flexible devices, photolithography process is indispensable for the large-scale integration (LSI) and down-scaling of devices. Of course, photolithography is possible to some polymer substrate, such as polyimide. Polyimide substrate has low transparency in visible range and high-cost. Thus, we employed parylene-C as a protection layer of PES substrate. Parylene-groups are generally used as the moisture barriers and the electrical insulators. Also, parylene has many advantages, such as hydrophobic, chemically resistant coating with good barrier properties for inorganic and organic media, strong acids, caustic solutions, gases, and water vapor.[5] Physical and chemical properties of poly (chloro-p-xylylene) or parylene thin films are attractive to use in many applications.[6] For some of these applications, the value of the permittivity is one of the important parameters to obtain the desired performance. Thus, parylene-groups are integrated for gate dielectric in organic field-effect transistors (FETs) to prevent ionic impurities in high-*k* material, to obtain a better immunity to ambient conditions (moisture, etc.), and finally to improve electric characteristics.[7–12] Parylene is produced in following three variations: parylene-N, parylene-C, and parylene-D, each suited to the requirements of a category of applications. Parylene-C is most widely used polymer, providing a useful combination of properties, plus a very low permeability to moisture, chemicals, and other corrosive gases. Parylene-N provides high dielectric strength and a dielectric constant that does not vary with changes in frequency. Best selection where greater coating protection is required. Parylene-D maintains its physical strength and electrical properties at higher temperatures. In this work, we designed the substrate employing SiO_2/parylene-C/PES structure. Parylene-C is used as the preventing layer to the solvent and the acid, and the SiO_2 capping layer is used for enhance the surface adhesion property. We demonstrated patterns with a few micrometers and fabricated the a-IGZO TFTs by using conventional photolithography process and wet-process on the substrate.

PES substrates are cleaned by isopropyl-alcohol and deionized water in the ultrasonic bath, respectively. Parylene-C layer of 100 nm is deposited by using the parylene coater on the PES substrates. And then, SiO_2 layer of 100 nm was deposited by using the plasma enhanced chemical vapor deposition (PECVD) at 150 °C. And then, we prepared two following samples to observe the difference: first sample (S1) is PES substrate encapsulated by parylene-C (parylene-C/PES) and another sample (S2) employed SiO_2 capping layer on PES substrate encapsulated by parylene-C (SiO_2/parylene-C/PES). On the substrate, we fabricated the a-IGZO TFTs. As a gate-electrode, Mo of 100 nm is deposited by direct current (dc) magnetron sputtering. And then, SiO_2 of 200 nm is deposited by PECVD. As the active layer, a-IGZO of 80 nm is deposited by radio frequency (rf) sputtering method using IGZO target (1:1:1 mol %). Basal vacuum is lower than 1.0×10^{-6} Torr and working pressure is maintained 10.0×10^{-3} Torr while the active layer is deposited. Substrate temperature and rf-power density are maintained at room-temperature and 1.85 W/cm^2, respectively. As the source/drain electrodes, Mo of 100 nm is deposited by dc-magnetron sputtering. Typically, it is not allowed to the conventional photolithography and wet-process

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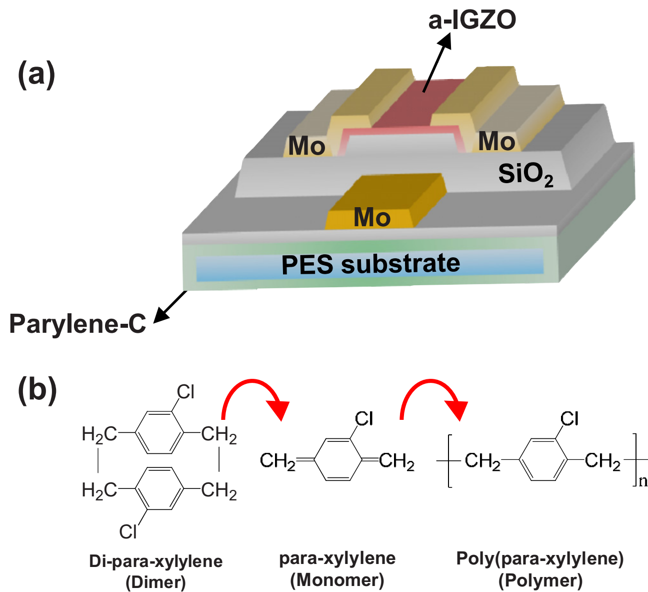

FIG. 1. (Color online) (a) The schematic diagram of a-IGZO TFT on the structure of SiO_2/parylene-C/PES substrate. Parylene-C is used to protect PES substrate from organic solvents and acids. Also, SiO_2 is used as the adhesive layer. (b) Deposition process of parylene-C.

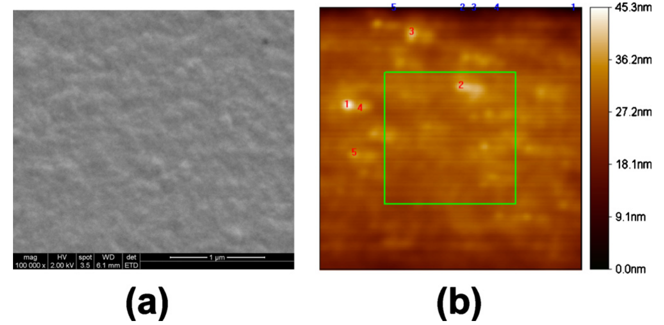

FIG. 2. (Color online) (a) SEM image and (b) AFM image of the surface of parylene-C on the PES substrate. The surface roughness of the parylene-C is confirmed to be about 2 nm by AFM.

on the PES substrate using solvents and acids. However, in our designed structure, we could demonstrate the TFT on the substrate by using the conventional photolithography, wet-process, and lift-off process. After make a device, annealing process is performed at 200 °C for 2 h in quartz tube furnace. N_2 is used as the ambient gas. In photography process, light source used is i-line ($\lambda = 365$ nm). Photoresist and developer are used to AZ 5214 and AZ CD-30, respectively. We performed conventional photography process. Finally, parylene-C surface on PES substrate is analyzed by using scanning electron microscope (SEM) and atomic force microscope (AFM). Also, electrical characteristics are measured by semiconductor parameter analyzer (Keithley 4200 SCS).

Figure 1 shows the schematic diagrams of SiO_2/parylene-C/PES substrate and a-IGZO TFT on the substrate. Because of PES substrate could be damaged by organic solvents and acids, TFTs on the flexible substrate are fabricated by using the metal-shadow mask. In order to improve the weakness of plastic substrate, we employed the parylene-C protection layer. However, because of parylene-groups have hydrophobic property, some adhesion layer is necessary to make a device. Thus, we choose the SiO_2 thin film of 100 nm as the adhesion layer for the fabrication of devices. Figure 2(a) shows SEM image of coated parylene-C on the PES substrate. The surface roughness of parylene-C surface is very smooth, and it could be confirmed in surface analysis evaluated by AFM measurement as shown in Fig. 2(b). In AFM analysis, surface roughness is measured to be about 2 nm. Figure 3(a) shows the SEM image of patterned electrode on the parylene-C/PES substrate. It seems like to be formed the pattern, however, detached part of the electrode is observed caused by hydrophobic property of parylene-groups as mentioned previously. Figure 3(b) shows the SEM image of patterned electrode on the SiO_2/parylene-C/PES substrate. In Fig. 3(b), well attached electrodes are observed caused by changed surface property from hydrophobic to hydrophilic via SiO_2 deposition. As a result, PES substrate is well protected by parylene-C thin film PES substrate from chemical reaction between PES substrate and organic media, and SiO_2 well performed to improve the adhesion of the substrate.

Figure 4(a) shows the output characteristics of a-IGZO TFT on the SiO_2/parylene-C/PES substrate. In Fig. 4(a), it is observed that device is operated with n-channel enhancement mode. Also, transfer characteristics of a-IGZO TFT on the SiO_2/parylene-C/PES substrate is shown in Fig. 4(b). The on-to-off current ratio was measured to be about 7.62×10^4 for the operation in the saturation region. The threshold voltage was defined by the gate-voltage, which induces a drain current of $W/L \times 10$ nA at a V_{DS} of 10.1 V.[4] Also V_{th} is estimated to about 19.7 V. The following is the expression for the estimation of carrier concentration.

$$N_{CH} = \frac{(V_{on} C_i)}{q t_{CH}}, \quad (1)$$

where q is the elemental charge quantity (1.6×10^{-19} C), t_{CH} is the thickness of active layer, V_{on} is the turn-on voltage of the device, and C_i is the capacitance per unit area of the gate-insulator. The carrier concentration of active layer is calculated to be 2.02×10^{17} cm^{-3} about by Eq. (1). The field-effect mobility and threshold voltage are calculated by linearly fitting the square root of I_D versus V_G curve of the transistor operating in the linear region. The following is the expression for the operation of a FET in the linear region:[13]

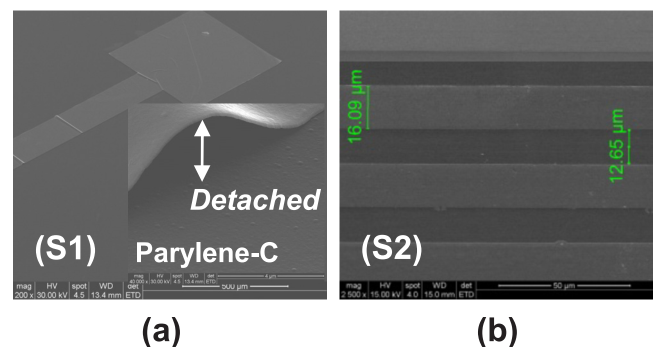

FIG. 3. (Color online) (a) SEM image of patterned electrode fabricated on the parylene-C/PES substrate (inset: it is observed that electrode is detached via the hydrophobic property of parylene-C). (b) SEM image of line patterns fabricated on the SiO_2/parylene-C/PES substrate.

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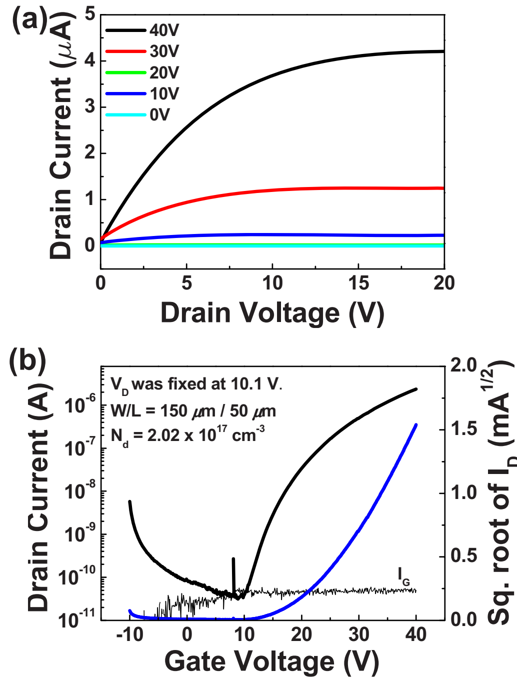

FIG. 4. (Color online) (a) Output characteristics and (b) transfer characteristics of a-IGZO TFT fabricated on the SiO_2/parylene-C/PES substrate. Device is annealed at 200 °C.

$$\mu_{FE} = \frac{g_m L}{W C_i V_D}, \tag{2}$$

where W is the channel width, L is the channel length, and g_m is the transconductance. The estimated field-effect mobility (μ_{FE}) in the linear region is 0.84 cm^2/V s. Generally, a-IGZO TFTs have been annealed at 300–350 °C. It means that enough activation energy is required to rearrange atoms within the a-IGZO thin film. In many research articles, the field-effect mobility of a-IGZO TFTs has been exhibited to be higher than 5 cm^2/V s. Also, in many case, annealing process is performed at over 300 °C.[3,4] However, the glass-transition temperatures (T_G) of PES substrate and parylene-C have been reported about ~220 °C, thereby annealing temperature could not be risen to over 200 °C in this work.[14,15] Thereby the mobility of a-IGZO TFT on the SiO_2/parylene-C encapsulated PES substrate is extracted to be 0.84 cm^2/V s caused by low annealing temperature. Also, in many research achievements, off-current of a-IGZO TFTs have the range from 10^{-13} to 10^{-11} A. Thus, we believed that the off-current of our device is reasonable. However, our device has low on-current of approximately microamperes caused by low annealing temperature of 200 °C. Although the electrical characteristics of our device is comparatively poor, we would like to suggests the possibility for adapting of lithography techniques to PES substrate in this work.

In summary, we designed the structure of SiO_2/parylene-C/PES substrate and demonstrated the a-IGZO TFTs on the substrate. We realized the photolithography technique on the PES substrate which could be damaged by reaction between PES substrate and organic solvents or acids. Of course, process temperature is limited by glass transition temperature of the PES substrate. However, this achievement is not only very useful to demonstrate a device on the PES substrate but also possible to realize the LSI of flexible electronic devices.

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