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The effect of annealing on amorphous indium gallium zinc oxide thin film transistors

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ABSTRACT

This paper presents the post-annealing effects, caused by rapid thermal annealing (RTA), on amorphous indium gallium zinc oxide (a-IGZO) thin film transistor's (TFT) electrical characteristics, and its contact resistance (R_C) with thermally grown SiO_2 gate dielectric on silicon wafer substrates. The electrical characteristics of two types of TFTs, one post-annealed and the other not, are compared, and a simple model of the source and drain contacts is applied to estimate the R_C by a transmission line method (TLM). Consequently, it has been found that the post-annealing does improve the TFT performances; in other words, the saturation mobility (μ_{sat}), the on/off current ratio ($I_{ON/OFF}$), and the drain current (I_D) all increase, and the R_C and the threshold voltage (V_T) both decrease. As-fabricated TFTs have the following electrical characteristics; a saturation mobility (μ_{sat}) as large as 0.027 $cm^2/V\,s$, $I_{ON/OFF}$ of 10^3, sub-threshold swing (SS) of 0.49 V/decade, V_T of 32.51 V, and R_C of 969 MΩ, and the annealed TFTs have improved electrical characteristics as follows; a μ_{sat} of 3.51 $cm^2/V\,s$, $I_{ON/OFF}$ of 10^5, SS of 0.57 V/decade, V_T of 27.2 V, and R_C of 847 kΩ.

1. Introduction

Currently, flexible and transparent electronic devices are the most promising field to realize the future-oriented technologies such as flexible display, solar cells, touch panel and wearable computings [1]. Thus, transparent thin film transistors (TFTs) are one of the key devices for achieving these products and these TFTs have been fabricated using oxide materials as active layers and transparent conducting oxides (TCOs) [2]. Until now, several binary, ternary, and quaternary oxide semiconductors have been selected and tested in recent years [3]. Among them, the amorphous indium gallium zinc oxide (a-IGZO), which is one of the most attractive materials, has been found to be appropriate for use as an active channel of TFTs because of its excellent electrical and optical characteristics [4–9]. The a-IGZO film has a wide bandgap and high transparency in the visible region as well as being able to be fabricated at low temperatures [10]. Because the *ns*-orbital of metal cation is larger than the *2p*-orbital of oxygen anion, the a-IGZO shows high mobility even though it has amorphous structure. In the case of fabricating TFTs on glass or plastic substrates, the process temperature is more important for manufacturing devices; accordingly, the a-IGZO has great potential to replace the existing silicon based semiconductors, such as polycrystalline and amorphous silicon, and organic based semiconductors, as an active layer of the TFT backplane of the flat panels and future generation displays [11–13]. Since Hosono et al. reported the fabrication of high performance a-IGZO based TFTs many researchers have also reported fruitful achievements in a-IGZO based TFTs [14,15]. Finally, these a-IGZO TFTs have shown excellent performances for realizing future displays, such as those demanding high mobility (>10 $cm^2/V\,s$), having flexible properties, and possessing transparency in the visible range [16]. In fabrication of a-IGZO based TFTs, the a-IGZO has been deposited by using radio frequency (rf) magnetron sputtering as an active channel. This technique generally provides such benefits as high deposition rates and has low processing temperatures [17]. However, in spite of these merits, the rf magnetron sputtering method occasionally results in lower TFT performances due to the increase in the surface morphology roughness. Because of the interface charge trap, scattering, and the contact resistance (R_C), a rough surface results in a decrease in the TFT's saturation mobility (μ_{sat}), the on/off current ratio, and the on drain current, as well as increasing the threshold voltage. To overcome these problems, the RTA is a very useful technique with many advantages, such as the short annealing time, and prevention of any strains or reactions at the film–substrate interface [18]. In this work, a-IGZO TFTs are prepared on a SiO_2/*p*-Si substrate. And then, in order to decrease the R_C, the RTA is performed on the device. Finally, the two devices are compared and analyzed: (a) a-IGZO TFT and (b) RTA treated a-IGZO TFT. By using these processes, a-IGZO based TFTs are fabricated on a SiO_2 gate dielectric, which has excellent performance.

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2. Experimental details

Fig. 1 shows a schematic cross section view of the TFT, which has been fabricated using phosphorous doped *p*-type silicon wafer with very low resistivity (ρ<0.005 Ω cm). The *p*-type Si wafer with low resistivity is used as the gate electrode. A 100-nm-thick SiO_2 layer is thermally grown on substrates by using a furnace (>1100 °C). These substrates are cleaned by acetone, methanol, and de-ionized water in an ultrasonic bath. As the active layer, an a-IGZO thin film of 50 nm is deposited using rf magnetron sputter at room temperature. The initial vacuum level is lower than 1×10^{-6} Torr and the working pressure and rf-power are maintained at 5 mTorr and 100 W, respectively during the sputtering. Before sputtering, pre-sputtering is performed to remove any contamination on the target surface, for 5 min. The active layer is patterned by conventional photolithography and a wet-etching process. Then, as the source/drain (S/D) electrodes, Ti of 10 nm and Au of 90 nm are deposited by e-beam and thermal evaporation, at room temperature. In this process, the basal vacuum is lower than 1×10^{-5} Torr, and the thickness is controlled by quartz thickness monitor. The S/D electrodes are patterned by conventional photolithography and a lift-off process. The channel width is designed to be 50 μm, and the channel length is varied from 2 μm to 200 μm. In this work, two devices have been fabricated: (a) an a-IGZO TFT without post-annealing, and (b) an a-IGZO TFT with post-annealing. The post-annealing process is performed in nitrogen atmosphere by using rapid thermal annealing equipment at 200 °C for 1 min. Also electrical characteristics of devices are measured by a semiconductor parameter analyzer (Keithley SCS 4200). Structural analysis and surface analysis have been performed by using atomic force microscopy (AFM, XE-100 system) and X-ray diffraction (XRD, Rigako D/MAX2200). Furthermore, the R_C is analyzed by the transmission line method (TLM).

3. Results and discussions

Figs. 2 and 3 show the electrical characteristics, expressed by plotting output and transfer curves for the two types of TFT devices, one with RTA and the other without. These TFTs have a 50 μm channel width and a 100 μm channel length. As shown in Fig. 2, both devices present the operation of a typical *n*-channel enhancement mode TFT [6]. A hard saturation is only seen in the output curve of annealed TFT. Fig. 3(a) and (b) shows the transfer characteristics of the as-fabricated and post-annealed TFTs, respectively. It is observed that a-IGZO TFT without RTA has a more unstable wide off-level range, and a higher threshold voltage (V_T) than the TFT with RTA. It is clearly seen that annealing one's characteristic is more suitable for TFT as a switching device, than another because of the resulting efficiency and stability. Table 1 shows a comparative list of the electrical characteristics of a-IGZO TFTs with and without post-annealing process. The V_T and μ_{sat}

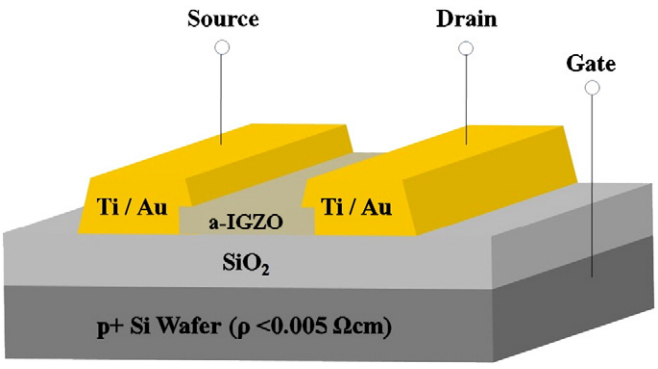

Fig. 1. Schematic cross section of the a-IGZO based TFT with SiO_2 gate dielectric on silicon substrates.

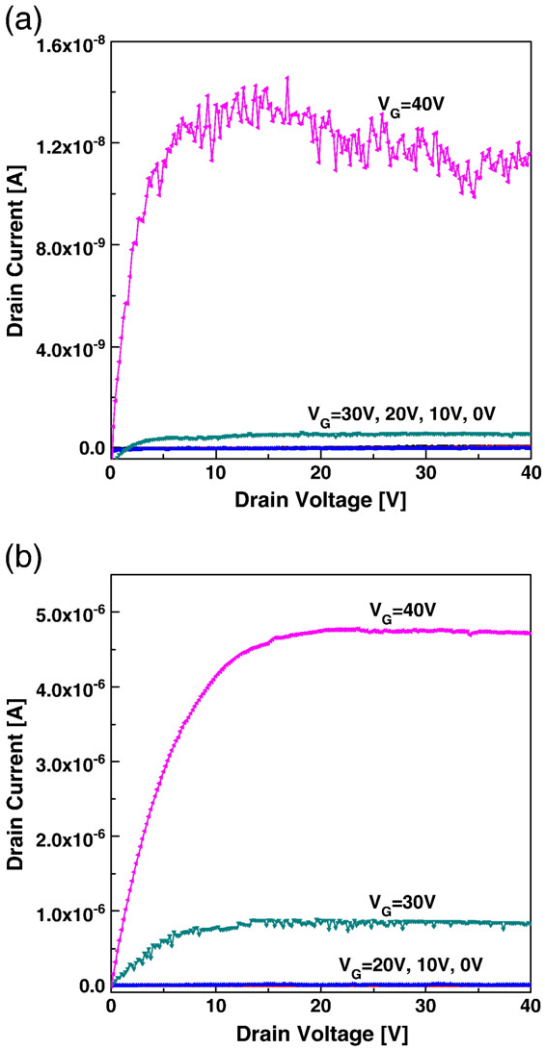

Fig. 2. Output characteristics of the a-IGZO based TFTs (a) with and (b) without post-RTA.

are estimated by linearly fitting the square root of the drain-source current (I_{DS}) versus the gate-source voltage (V_{GS}) curve in the saturation region. The following equation is the expression for the operation of a field effect transistor in the saturation region [19]:

$$I_{DS} = \left(\frac{C_i \mu_{sat} W}{2L}\right)(V_{GS}-V_T)^2 \text{ for } (V_{DS} > V_{GS}-V_T) \quad (1)$$

where W is the channel width, L is the channel length, and C_i is the capacitance per unit area of the gate insulator (around 34.5 nF/cm^2 for SiO_2 gate dielectrics). This result, caused by the RTA from a re-arrangement of the surface morphology, leads to a much improved interface condition between the active layer and the electrodes [20]. Thus, good interfacial condition brings improved electrical performances of a-IGZO TFTs, giving a higher on current and lower V_T, which is important in achieving a low voltage driven device. If the a-IGZO active channel has poor surface roughness, then this leads to valleys in the channel region, which may act as carrier traps with a number of scatterings [21]. Fig. 4(a) and (b) shows the AFM image of the TFT active channel, with and without RTA, respectively. The RTA effect is also recognized by using the AFM image which reveals the active channel surface morphology difference in each type of TFT. The TFT without RTA has a surface uniformity with a root mean square value (RMS) of roughness of 2.209 nm. On the other hand, the TFT with RTA has a RMS roughness of 1.270 nm. As mentioned previously, the RMS

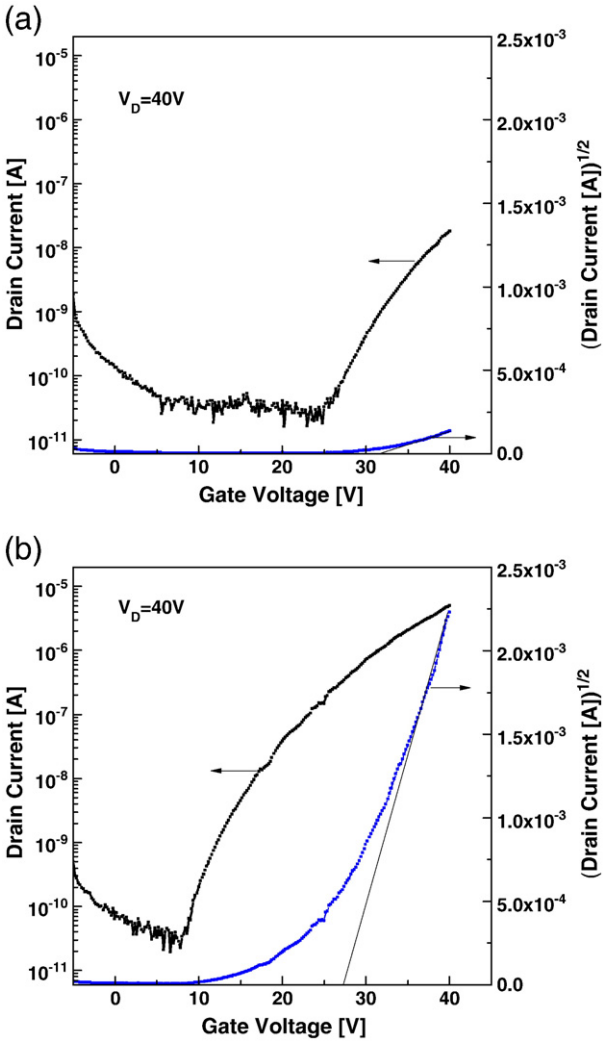

Fig. 3. Transfer characteristics of the a-IGZO based TFTs (a) without and (b) with post-RTA.

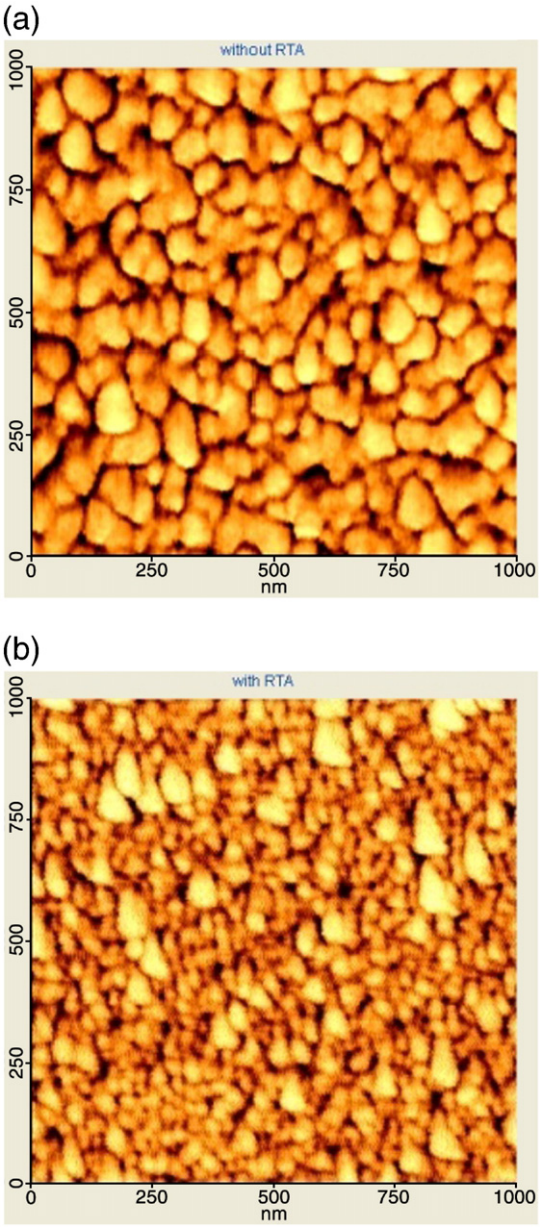

Fig. 4. AFM images of the IGZO film on the SiO_2 gate dielectric (a) without and (b) with post-RTA.

roughness value of the RTA treated TFT is lower than the value of the TFT without RTA. This means that the RTA treatment ensures a smoother active channel surface morphology. The smooth surface morphologies of the a-IGZO thin films can develop good interfaces for both the source and the drain electrode contact regions with the active channel [22]. If the a-IGZO thin film can be crystallized by RTA, the surface roughness will be increased owing to the formed grains. However, the reduced surface roughness means a non-crystallized a-IGZO thin film, and it is confirmed that the a-IGZO thin film maintains an amorphous phase, as shown in Fig. 5. The XRD patterns of the annealed a-IGZO films have only one peak, monopolized at 53°, which matches that of the $p+$ silicon. As a result, a-IGZO film's crystallinity is not influenced by RTA. The concentration of as-fabricated a-IGZO and RTA treated thin films is estimated to be about $1.0\times10^{18}\,cm^{-3}$ and $8.4\times10^{17}\,cm^{-3}$, respectively. Also, following is expression for the estimation of carrier concentration [24].

$$N_{CH} = \frac{(V_{on}C_i)}{qt_{CH}}\left[cm^{-3}\right] \tag{2}$$

where q is the unit charge quantity, and t_{CH} is the thickness of active layer. The carrier concentration within a-IGZO thin film is almost not changed by RTA treatment. So, the change of carrier concentration is negligible in terms of thin film characteristics. In case of a-IGZO thin film, thermal energy is required to rearrange atoms on the local sites. In other words, annealing temperature is attributed to internal modifications in the semiconductor structure leading to improved local atomic re-arrangement [23]. However, annealing temperature of 200 °C is not enough to fully rearrange atoms in a-IGZO thin film. This is because all devices have been exposed to temperature of about 150 °C while sputtering is performed. Therefore, the reduction of contact resistance is

Table 1
List of electrical characteristics of TFT, comparing the RTA process.

	Saturation mobility (μ_{sat}) [cm^2/V s]	On/off current ratio ($I_{ON/OFF}$)	Subthreshold swing (V_{SS}) [V/decade]	Threshold voltage (V_T) [V]
IGZO TFT Without RTA	2.71×10^{-2}	1.13×10^{3}	4.92×10^{-1}	32.51
IGZO TFT With RTA	3.51	1.89×10^{5}	5.73×10^{-1}	27.27

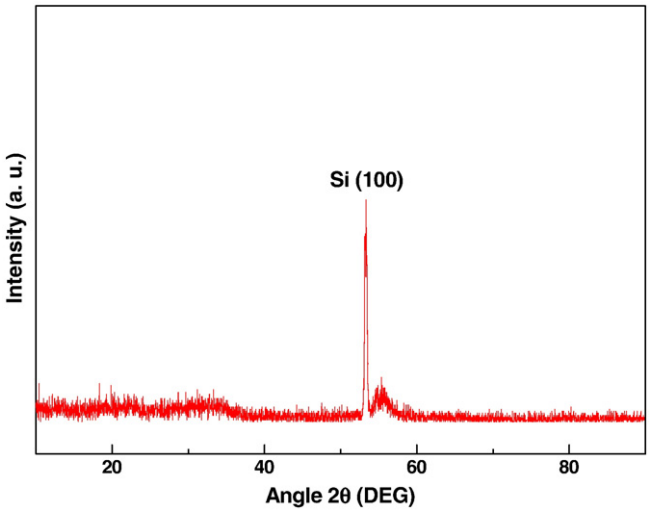

Fig. 5. X-ray diffraction patterns of the as-deposited a-IGZO thin film and after annealing at 200 °C on *p*-type silicon wafer.

a dominant factor to improve the device performance in this work. Finally, to verify annealing effects that make surface morphology smoother and improve TFT performance, we suppose that surface morphology makes contact resistance low. Thus, we calculate contact resistance by using TLM technique. To obtain the R_C of the active channel and electrodes, a simplified TFT structure is designed to a variety of channel lengths, ranging from 20 μm to 150 μm, and the resulting drain current measured for each case. Fig. 6(a) and (b) shows the inverse of the drain current as a function of the channel length for each TFT. It was assumed that as the source and drain contacts resistance is separated from the potential drop across the contacts, the contact resistance can be calculated by plotting the inverse of drain current versus channel length, extrapolating the *y*-axis intercept (where the channel resistance disappears), and multiplying by the drain-source voltage [25]. The resistance values for $V_G = 40$ V are approximately 847 kΩ with RTA, and 969 MΩ without RTA. (The total R_C is the sum of the source and drain R_C with the active layer). As a result, the RTA makes the surface roughness decreased that caused the R_C to decrease. Therefore, the TFT's electrical characteristics, such as the μ_{sat}, the on/off current ratio, and the V_T, are improved [20].

4. Conclusions

In this study, the electrical characteristics of two types of TFT, with and without RTA, are presented by plotting the output and transfer curves. By comparing these TFTs, the post-annealed TFT is found to be more suitable to be used for switching devices, and has better performances, such as higher μ_{sat}, larger currents and on/off ratios, as well as lower V_T, than others. The R_C has been analyzed by the TLM technique, and it has been found that the RTA leads to decreased R_C, thereby leading to improvement of the electrical characteristics of the TFT. In consequence, the RTA effect on a-IGZO TFT's electrical characteristics has been presented. Future work plans to fabricate a-IGZO TFTs on the plastic substrates. It is expected that this work will be useful in further advancing the oxide based TFT technology for future devices.

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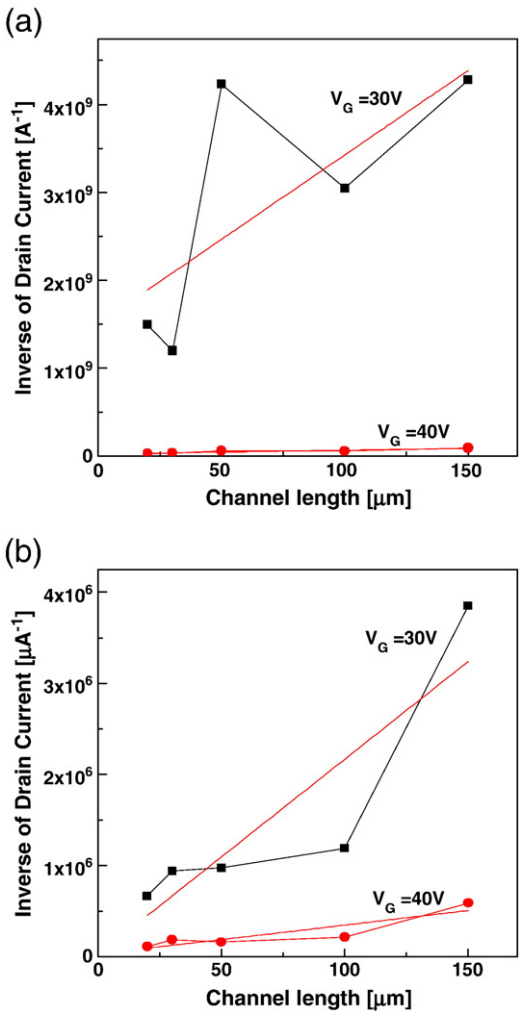

Fig. 6. Inversion of drain current as a function of the channel length for TFT (a) without and (b) with post-RTA.

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