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## Abstract

The effects of dielectric layer thickness on the electrical performance and photosensing properties of organic pentacene thin-film transistors have been investigated. To improve the electrical performance of pentacene thin-film transistors (TFTs), the poly-4-vinylphenol (PVP) polymer with various thicknesses was used in fabrication of the pentacene

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ABSTRACT

The effects of dielectric layer thickness on the electrical performance and photosensing properties of organic pentacene thin-film transistors have been investigated. To improve the electrical performance of pentacene thin-film transistors (TFTs), the poly-4-vinylphenol (PVP) polymer with various thicknesses was used in fabrication of the pentacene transistors. The pentacene thin-film transistor with the PVP dielectric layer of 70 nm exhibited a field-effect mobility of 4.46 $cm^2/Vs$ in the saturation region, a threshold voltage of −4.0 V, a gate voltage swing of 2.1 V/decade and an on/off current ratio of $5.1 \times 10^4$. In the OFF-state, the photoresponse of the transistors increases linearly with illumination intensity. The pentacene transistor with the thinner dielectric layer thickness indicates the best photosensing behavior. It is evaluated that the electrical performance and photosensing properties of pentacene thin-film transistors can be improved by using various thickness dielectric layer.



## 1. Introduction

There has been great interest in thin-film transistors of organic materials, since organic thin-film transistors (OTFTs) have many unique advantages, such as light weight, flexibility, and solution processability. From these reasons, nowadays, many research groups have developed OTFTs. Especially, solution processes included spin coating [1], screen printing [2], drop casting [3], and nanoimprint lithography [4] can be easily used in coating processes to form circuits for disposable electronics on a plastic substrate. According to the reported investigation of active channel pentacene is a very promising candidate for organic electronics [5]. Several groups have recently demonstrated pentacene TFTs and their applications [6,7]. However, to satisfy the high performance of OTFT, it is very important to select a gate insulator material. That is, an insulator gate field-effect transistor, the role of the insulator is at least as important as that of the semiconductor. Also, the insulator layer, especially the insulator–semiconductor interface, has a significant effect on the performance of OTFTs, because OTFTs operate in accumulation region and the modulated charge lies within the area (about 10 nm thick) close to the interface [8]. Therefore, many research groups have made much effort to be study on relationship between organic semiconductor and dielectric layer.

Of many organic dielectrics, solution processable poly-4-vinylphenol (PVP) is a good candidate because of its slightly higher $k$ and stable cross-linking properties [8]. Moreover, Byun and his coworkers reported that use of PVP as gate dielectric in pentacene OTFT achieves the overall best performances [9].

In present work, we have prepared a process of using PVP as gate insulator to fabricate pentacene OTFT. Furthermore, to optimize the deposition of the PVP gate dielectric in our devices, we compared the devices as varying dielectric thickness, measured and analyzed the performance of photoresponse as varying illumination intensity.

## 2. Experimental

OTFT was fabricated with the widely used bottom-gate and top contact geometry as shown in Fig. 1. 100-nm-thick indium tin oxide (ITO, sheet resistance ~10.0 ohm/sq) layer was deposited on a glass substrate by the sputtering evaporation. Next, a cross-linked PVP film served as a gate dielectric. To make the gate dielectric layer, our devices are prepared with different composition of dielectric material to confirm the effect of thicknesses of dielectric layer in device performance. Therefore, the poly-4-vinylphenol (PVP) powder (Sigma–Aldrich, Mw ~20,000) was mixed with 3, 8, and 13 wt.% of propylene glycol monomethyl ether acetate (PGMEA), individually, and then we added the cross-linking agent, poly(melamine-co-formaldehyde) (Sigma–Aldrich, Mw ~511), to the PVP solution with a ratio of 1:20. To form a PVP dielectric film,

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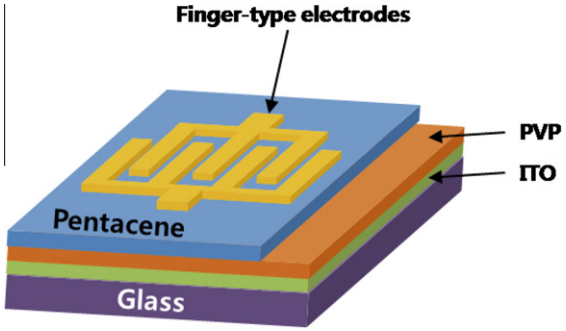


**Fig. 1.** Schematic structure of OTFT.

**Table 1**
The parameters of the OTFTs.

| OTFT | PVP (3 wt%) | PVP (8 wt%) | PVP (13 wt%) |
|---|---|---|---|
| Substrate | ITO glass | ITO glass | ITO glass |
| Thickness(nm) | 70 | 240 | 540 |
| $\mu$ ($cm^2$/Vs) | 4.46 | 1.5 | $2.3 \times 10^{-4}$ |
| $V_{th}$ (V) | −4 | −6.2 | 5 |
| $S$ (decade) | 2.1 | 6.1 | 9 |
| On/off ratio | $5.1 \times 10^4$ | $1.1 \times 10^2$ | 8 |

the PVP solution was coated on the glass substrate with an ITO electrode and a curing process was conducted at 200 °C for 10 min on a hot plate to enforce the cross-linking of the PVP polymer. Subsequently, a 70 nm thick pentacene (Sigma–Aldrich, ~99% purity) active layer was deposited on the different dielectrics with a deposition rate of 0.4 Å/s under a base pressure of $1 \times 10^{-6}$ Torr by a thermal evaporator (DOV Co., Ltd.). The thicknesses of the PVP dielectric layer were determined to be 70 nm, 240 and 540 nm, respectively. Here, measurements of the film thickness are done by a surface profilometer (Tencor, Alpha-step 500). Finally, the 200 nm thick Au source and drain electrodes were deposited through a shadow mask by the thermal evaporator. The channel width and length were 2500 and 100 μm, respectively. The thickness of PVP layer for the transistors is given in Table 1. Schematic structure of OTFT is shown in Fig. 1. The transistor characteristics of the transistor were measured by using a semiconductor characterization system (Keithley SCS 4200) in a dark box. Photovoltaic measurements were employed using a 200 W halogen lamp. The morphology of the dielectric layer was examined with a Solver P47H Atomic Force Microscope operating in tapping mode in air at room temperature.

## 3. Results and discussion

We modified the thickness of the poly-4-vinylphenol dielectric layer to improve the photovoltaic properties of pentacene thin-film transistor. The film properties of dielectric layer were investigated by AFM. The two-dimensional and three-dimensional atomic force microscopy (AFM) images of dielectric layer with having various thicknesses are shown in Fig. 2 and 3. The roughness of the PVP-70 nm, PVP-240 nm and PVP-540 nm dielectric layers is changed by the thickness of dielectric layer and the rms (root mean square) roughness of PVP-70 and PVP-240 nm films are almost the same. The rms roughness values of PVP-70 nm, PVP-240 nm and PVP-540 nm dielectric layers were found to be 0.018, 0.017, and 0.18 nm, respectively, and the bright areas in the images have been interpreted as regions of increased film thickness, as shown in Fig. 3a–c. But, clearly see that there is a big difference in between PVP-240 and PVP-540 nm films. The surface roughness of the PVP dielectric layer have an important effect on the performance of the organic phototransistor, since the charge carrier transport in the active layer is affected by the dielectric layer morphology.

Figure ure4 shows the drain current–voltage characteristics for transistors fabricated using 70, 240 and 540 nm dielectric layer, respectively. As seen in Fig. 4, the drain-source current of the transistor increases with negative gate voltages. This suggests that the thin-film transistor indicates a clear p-channel transistor behavior. At lower voltages, the drain current–voltage curves exhibit good linearity of response. This confirms that a good Ohmic contact was established between the pentacene and gold contacts [10].

The drain current–voltage characteristics of OTFTs can be analyzed by the following relations [11–13],

$$I_{ds} = \frac{W}{L}\mu C_i\left[(V_g - V_{th})V_d - \frac{V_d^2}{2}\right] \quad \text{for linear region} \tag{1}$$

and

$$I_{ds} = \frac{W}{2L}\mu C_i(V_G - V_{th})^2 \quad \text{for saturation region} \tag{2}$$

where $I_{ds}$ is the drain-source current, $W$ is the width of channel, $L$ is the channel length, $C_i$ is the capacitance per unit area of the insulator. $V_g$ is the gate voltage, $\mu$ is the mobility and $V_{th}$ is the threshold voltage. The electrical parameters, i.e., off-current, threshold voltage, and field-effect mobility, of the transistors are determined and are given in Table 1. The field-effect mobility,

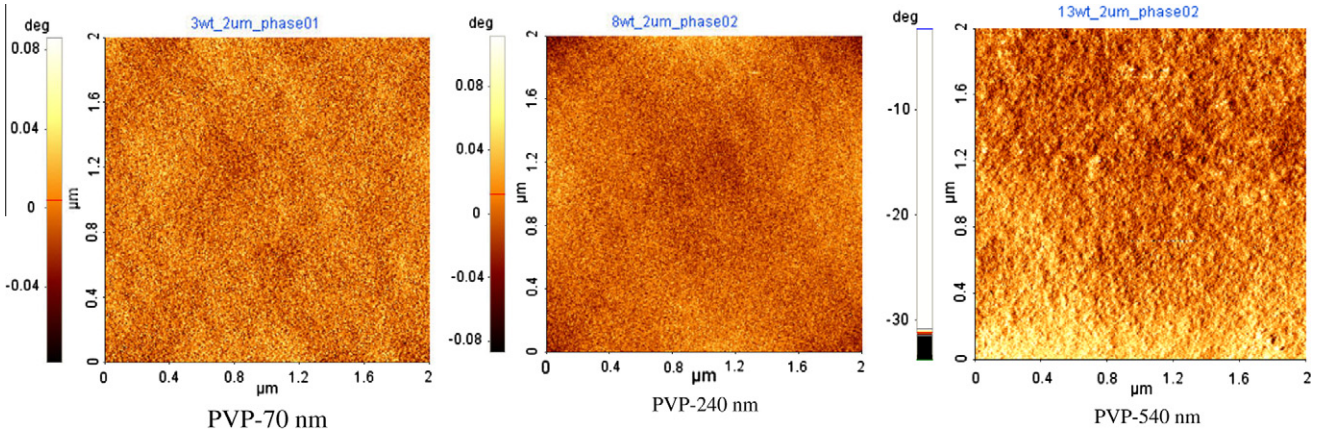


**Fig. 2.** Two-dimensional AFM images of PVP dielectric layer having various thicknesses.

threshold voltage, on/off ratio of OTFTs from $I_{ds}^{1/2} - V_g$ plot were found and are given in Table 1. As seen in Table 1, the mobility of OTFTs increases with decrease in dielectric layer. We have evaluated that the surface roughness and dielectric layer thickness is effective parameters on the performance of the transistors. As seen in Fig. 3, the roughness of dielectric layers of 70 and 240 nm is almost the same. This indicates that the thickness of the gate layer is important parameter on mobility of the transistors. The decrease in thickness of the gate layer enhanced the charge transport characteristics. The transistor with dielectric layer of 70 nm gives the best mobility value (4.46 $cm^2$/Vs) with surface roughness of 0.018 nm. The mobility (4.64 $cm^2$/Vs) value of the pentacene of 70 nm transistor with PVP dielectric gate layer of 240 nm with 0.018 nm roughness is higher than that of the mobility (1.64 $cm^2$/Vs) value of the

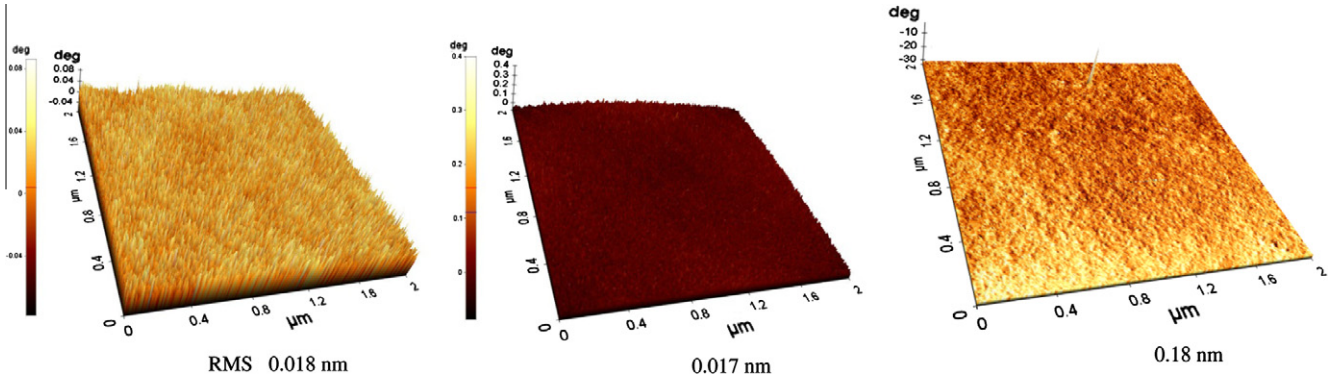


**Fig. 3.** Three-dimensional AFM images of PVP dielectric layer having various thicknesses.

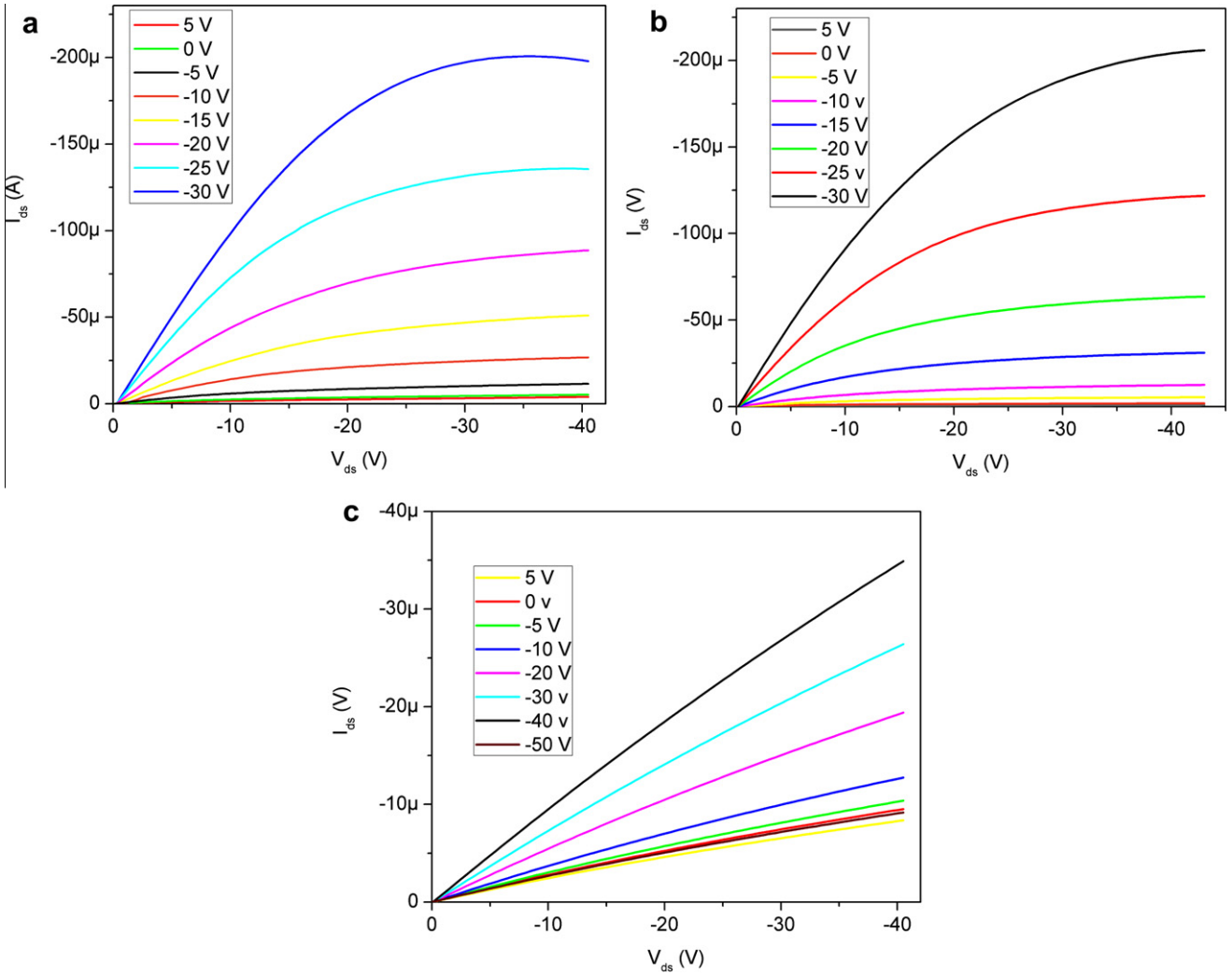


**Fig. 4.** Plots of $I_{ds} - V_{ds}$ of OTFTs under various gate voltages (a) PVP-70 nm (b) PVP-240 nm (c) PVP-540 nm.

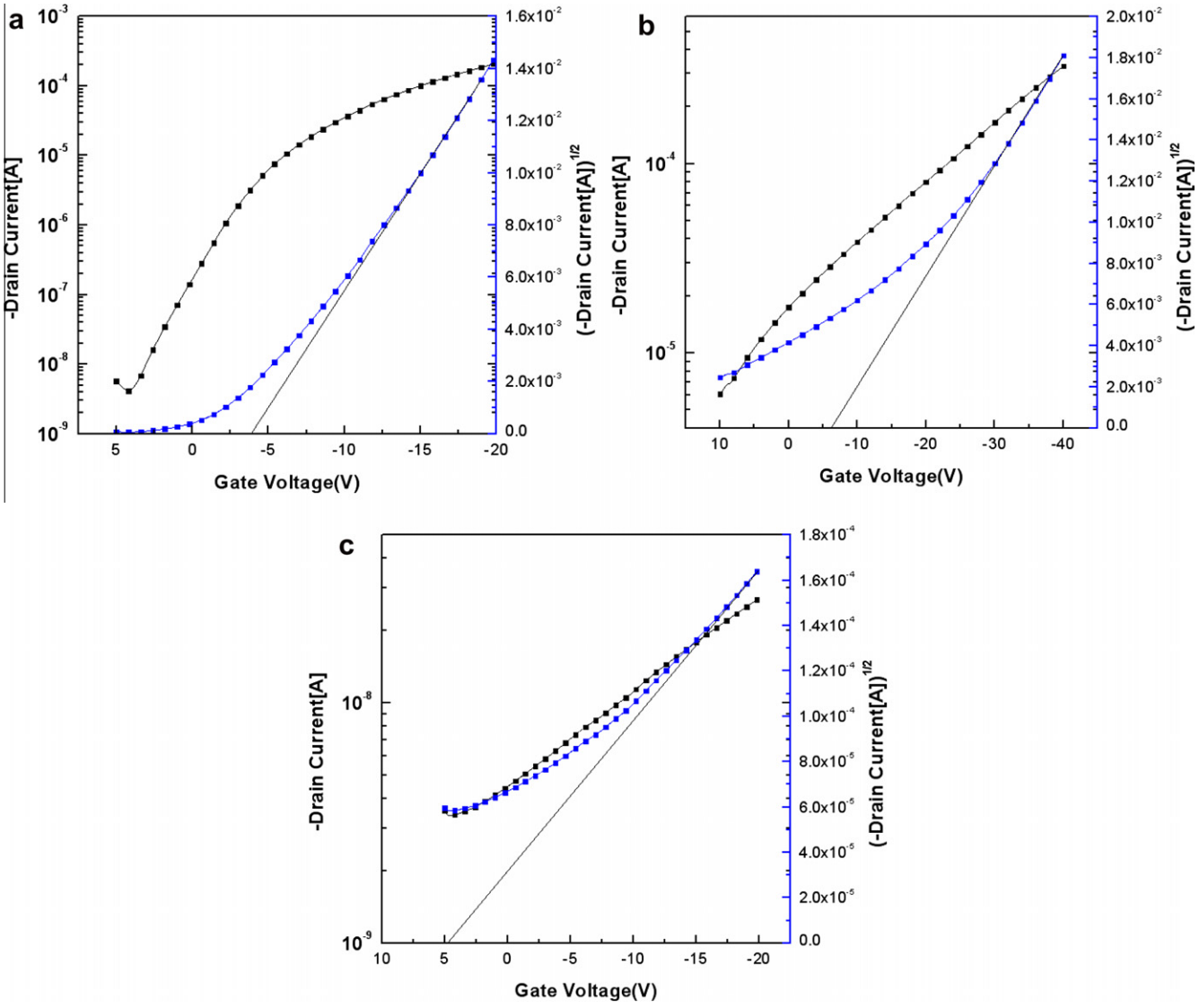


**Fig. 5.** Plots of −drain current − $V_g$ and (−drain current)$^{1/2}$ − $V_g$ of OTFTS. (a) PVP-70 nm under $V_{ds}$ = −20 V (b) PVP-240 nm under $V_{ds}$ = −40 V (c) PVP-540 nm under $V_{ds}$ = −20 V.

pentacene of 70 nm transistor with PVP dielectric gate layer of 240 nm with roughness of 0.347 nm [7] and furthermore, it is higher than that of the mobility (1.14 $cm^2$/Vs) of pentacene thin-film transistor with polymethyl-methacrylate-co-glyciclyl-methacrylate (PMMA–GMA) dielectric layer [14]. This indicates that the roughness of dielectric layer enhanced the performance of the transistor, because the mobility in thermally grown pentacene on a dielectric film is influenced by the π-orbital overlap between neighboring pentacene molecules [15]. The higher mobility reported for pentacene layer could be due to a higher conductivity of crystalline phase forming domains extending from source to the drain as in a network of parallel resistances (dominated by the most conductive ones). Also, it is well known that an OTFT device functionality strongly depends on the morphology of the semi-conducting layer which is mainly affected by the surface properties of the underlying layers of the gate dielectric, so a smooth dielectric–semiconductor interface is essential for efficient transport in the OTFT channel [16–18]. If the dielectric film has poor surface roughness, then this roughness leads to valleys in the channel region, and these valleys may act as carrier traps with a number of scatterings [15].

Furthermore, in an OTFT, the gate voltage switches the transistor with insulator thickness and dielectric constant. The obtained results indicate that the performance of the pentacene transistor improved by the surface roughness and lower thickness of the PVP dielectric layer. The on/off ratios of the transistors were calculated and are given in Table 1. The on/off ratio of the transistors is decreased with increase in thickness of dielectric layer. The on/off ratio for the transistor of 70 nm dielectric layer was found to be $5.1 \times 10^4$ and this parameter is one of the important OTFT parameters that determine device quality.

The threshold voltage values of the transistors were determined and are given in Table 1. The threshold voltage of the transistors was increased from −4 to 5 V with increasing thickness of dielectric layer. This indicates that the threshold voltage is improved by using a thinner gate insulator and in turn, the transistor works at good performance. The higher threshold voltage is attributed to the density of bulk trap states inside dielectric layer. It is observed that the $V_{th}$ values change from negative to positive. This shifting can be due to higher capacitance of gate dielectric. Furthermore, the increase in $V_{th}$ is attributed to hole accumulation. The hole accumulation on the conduction channel can tune the highest

occupied molecular level and in turn, the threshold voltage is decreased with the decrease in the thickness of the dielectric layer.

Another important parameter of OTFTs is the inverse sub-threshold slope S and it can be determined from the plot of $\log I_{ds}$ versus $V_g$, because $S$ value of the transistor controls the voltage swing that is required to turn a transistor from "off" to "on" state. The $S$ values were calculated from Fig. 5 and are given in Table 1. The transistor with the dielectric layer of 70 nm has the lowest $S$ value of 2.1. The $S$ value of the present transistor is lower than that of pentacene transistor proposed in literature [7]. We evaluate that the studied transistor exhibits better performance with a smaller $S$ value.

The sub-threshold behavior of the drain current is attributed to the distribution of defect states in the band gap. The maximum number of present interface traps can be calculated by the following relation [19],

$$D_{it} = \left[\frac{S\log(e)}{kT/q} - 1\right]\frac{C_i}{q} \tag{3}$$

where $k$ is the Boltzmann constant, $T$ is the temperature and $q$ is the electronic charge. The $D_{it}$ values for the transistors were found to be $10.85 \times 10^{12}\ eV^{-1}cm^{-2}$ for 70 nm, $9.40 \times 10^{12}\ eV^{-1}cm^{-2}$ for 240 nm and $6.16 \times 10^{12}\ eV^{-1}cm^{-2}$ for 540 nm, when the thickness of the PVP dielectric layer is varied. The highest $D_{it}$ value was found for the lowest thickness of the PVP dielectric layer. This indicates that the pentacene transistor with $10.85 \times 10^{12}\ eV^{-1}cm^{-2}$ exhibited improved electrical characteristics, because the high $D_{it}$ value makes a contribution to the capacitance of the dielectric layer and in turn, the mobility of the transistor increases.

In order to determine the photosensing characteristics of the transistors, the drain-current plots of the pentacene thin-film transistors with various dielectric thicknesses under various illumination conditions were measured and are shown in Fig. 6. As seen in Fig. 6, the drain-source current of the transistor increases with illumination, because the illumination increases the flow of mobile carriers in the channel layer. The photosensing behavior of the pentacene transistors changes with the dielectric layer thickness. The dielectric layer with various thicknesses performs excellent light scattering behavior. Thus, the thinner dielectric layer enhances photosensitivity due to the photocurrent created between source and drain of the pentacene OTFT.

The photoresponse of the transistors can be analyzed by the following relation [20],

$$R_{L/D} = \frac{I_{\text{illumination}}}{I_{\text{dark}}} \tag{4}$$

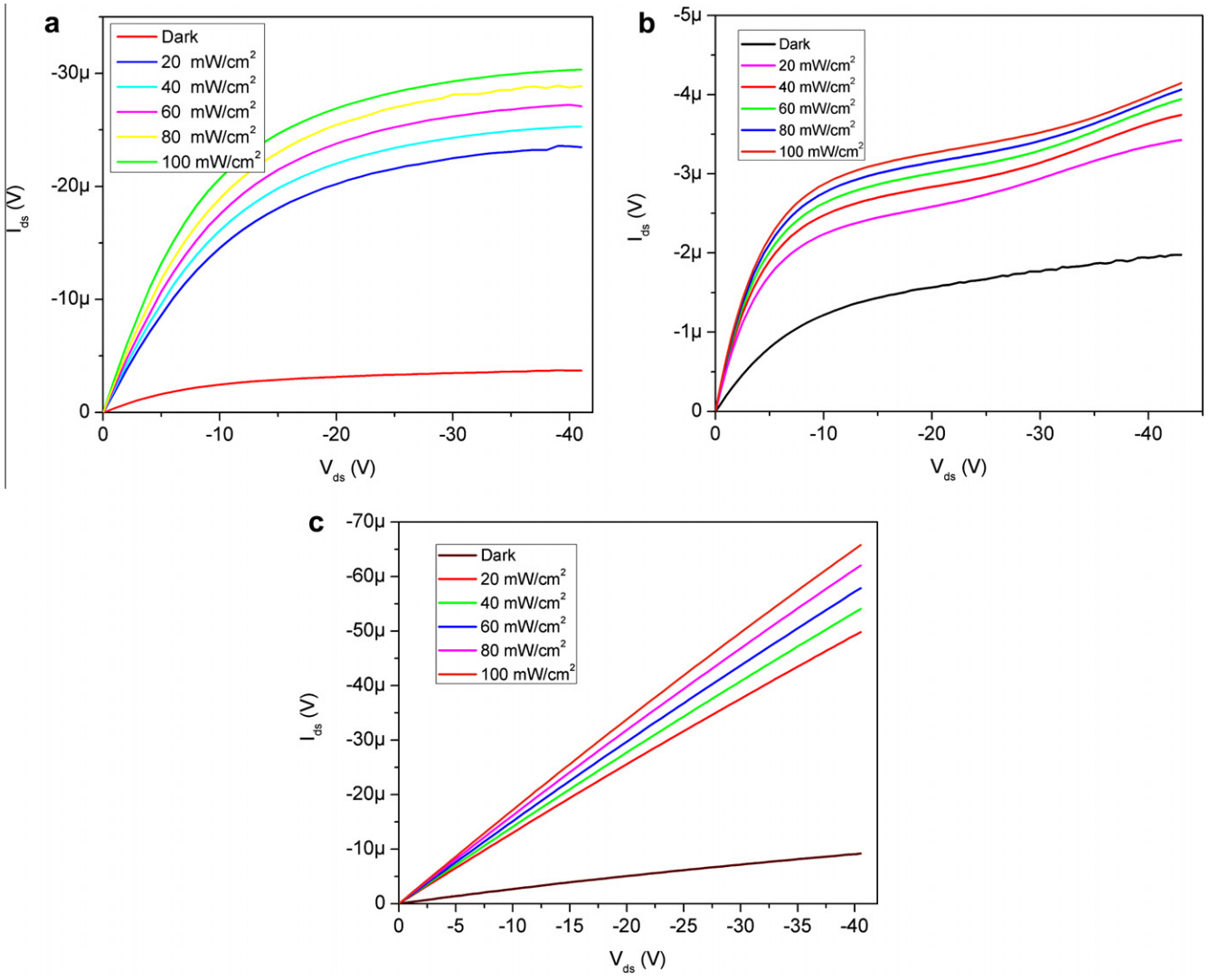


**Fig. 6.** Plots of $I_{ds} - V_{ds}$ of OTFTs under various illuminations for $V_g = 0$ V (a) PVP-70 nm (b) PVP-240 nm (c) PVP-540 nm.

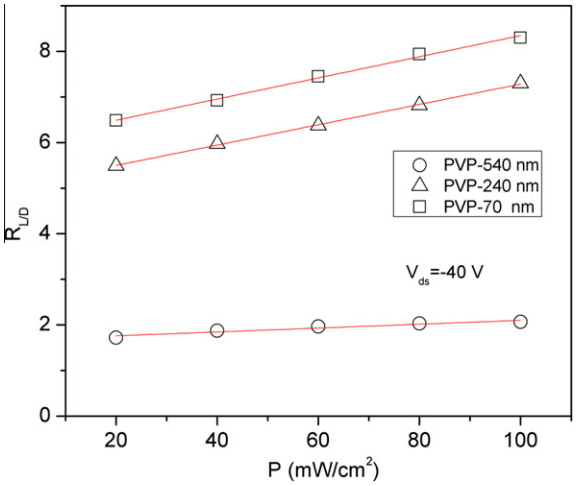


**Fig. 7.** Plots of $R_{L/D} - P$ of OTFTs under $V_{ds} = -40$ V.

where $I_{illumination}$ is the drain-source current under illumination and $I_{dark}$ is the drain-source current under dark. The $R_{L/D}$ values dependence of illumination intensity of the pentacene phototransistors are shown in Fig. 7. As seen in Fig. 7, in the OFF-state, the photoresponse of the transistors increases linearly with illumination intensity. The pentacene transistor with the thinner dielectric layer thickness indicates the best photosensing behavior.

This suggests that the photosensing properties of pentacene thin-film transistors can be controlled by using various thickness dielectric layer. We have evaluated that the gate voltage switches the OTFT with insulator thickness and dielectric constant. The obtained results indicate that the dielectric layer of low thickness improves the photosensing properties of the OTFTs, because, the dielectric surface impacts the charge – trapping density and growth of the active organic layer deposited on top of it. The high capacitance value of the dielectric layer makes a contribution to interface state density and charge-trapping density, resulting in a strong increase in the photosensing properties.

The pentacene transistor having the lowest thickness of the PVP dielectric layer with $10.85 \times 10^{12}$ $eV^{-1}$ $cm^{-2}$ exhibited the highest photosensing behavior, because, the distribution of trapped photocarriers depends on the distribution of defects. Photo-generated holes are easily trapped by the lower energy defects near the interface [21]. Therefore, after turning off the illumination, the trapped electrons are de-trapped, and resulting in the number of carrier charges in the organic semiconductor smaller than the original value [21]. More charges can be trapped in the trap states with increasing exposure time and in turn, the photo-generated charges contribute to the drain current, resulting in a strong increase in the drain current.

## 4. Conclusions

To improve the electrical and photosensing performance of pentacene thin-film transistors, we employed the various thickness of PVP dielectric film. The obtained results indicate that the good surface morphology and the lower film thickness of the PVP dielectric layer improved the electrical performance of the pentacene TFTs.

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