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Fabrication of oxide thin film transistor based on SOG dielectric and solution ZnO

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ZnO TFTs use less vacuum processes. SiO_2 as a dielectric layer was formed on a silicon and glass substrate using a spin on glass (SOG). On top of the SiO_2 layer, ZnO thin films were spun using sol-gel method from an IPA solution of zinc acetate dehydrate stabilized by 2-aminoethanol. Thus, it was necessary to make the surface of the SiO_2 hydrophilic coating process (ZnO layer) using RIE system. In the last process, sources and drain electrodes were made from N-type metal (Mo) using dc-sputtering. In order to analyze the characteristics of the fabricated device, X-ray diffraction (XRD), scanning electron microscopy (SEM), Contact Angle analysis, and differential scanning calorimetry (DSC) & thermogravimetry (TG) were applied, and the current-voltage (I-V) characteristics of these TFTs were measured by semiconductor parameter analyzer characterization systems.

Key words: Oxide TFT, Solution process, SOG, ZnO.

Introduction

There is currently significant interest in realizing high performance thin-film transistors (TFTs) based on solution-processible semiconducting materials for applications requiring low-cost, large scale manufacturing on rigid or flexible substrates. Thus, much effort has been devoted to high performance solution-processible semiconductors as a potential alternative to traditional vacuum system semiconductors. However, solution-processible semiconductors have generally been made using applied organic materials because organic materials are flexible and may be formed at low temperatures. However, OTFTs developed thus far have not yielded high performance. As a result, there have recently arisen various approaches to realizing solution-processible inorganic semiconductors, which provide a potential route to significant performance gains. Inorganic semiconductors might provide a route to high performance n-type TFTs required for complementary circuits, which are traditionally difficult to realize with organic TFTs.

The production of performance solution-processed semiconductor films represents a challenge to key materials, potentially enabling a wide range of applications [2-8]. ZnO is a non-toxic inorganic semiconductor which potentially offers salient features such as high mobility, excellent environmental stability and high transparency. One possible application of ZnO TFTs involves their use as transparent select transistors in each pixel of an active-matrix liquid-crystal display (AMLCD). An important measure of TFT performance for these types of applications is the magnitude of the electron channel mobility. A higher mobility leads to a higher drive current and faster device operating speeds, which translates into more application possibilities.

We investigated the solution-processing technique for the deposition of spin on glass (SOG) with TFT [9] and then investigated in high-mobility ZnO films which should be important for efficient charge transport and high FET mobility. In this paper, the major issue is that fabrication of the ZnO TFTs adapted solution process via the spin-coating precursor solution onto substrates. Also, we adjust the SOG process of previous study. Thus, the necessary vacuum equipment was reduced.

Device Structure

A 1 : 1 molar solution of zinc acetate dehydrate : isopropyl alcohol (IPA) in 2-methoxyethanol (MEA) was prepared as the ZnO precursor solution for our studies. Different concentrations of the precursor solution were prepared by dilution with 2-methoxyethanol. Bottom-gate, top-contact TFT test devices were fabricated on silicon substrate coated with ~150 nm sputtered molybdenum (Mo) layer and ~800 nm layer of SiO_2 applied by SOG. The Mo and SiO_2 layers constituted, respectively, the gate electrode and the gate dielectric of the device. For a solution-processable gate dielectric, we utilized a siloxanebased SOG (Honeywell 512B, dielectric constant = 3.1 ± 0.1) that was composed primarily of siloxane that contained CH3 (15% organic content) groups bonded to Si atoms in the Si-O backbone. The SOG was spin-coated on the HF-treated Si surface at a spin rate of 5000 rpm/min for 20 s, baked successively at 80 °C and 250 °C for 1 min each in air, and finally, cured at 600 °C in 1.0 L·min-1 N_2 flow. For the spin-coated

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ZnO film, a 0.05 M zinc acetate dihydrate : IPA (1 : 1) solution in 2-methoxyethanol was spin coated at a speed of 3500 rpm on top of the SiO_2 layer, preheated on a hot plate at 300 °C and then cured at 500 °C in air. Before spin coating of the ZnO, the SiO_2 layer was made hydrophilic to ease coating for a more uniform surface using O_2 plasma treatment. Finally, source/drain electrodes (Mo) were mounted on top of the ZnO layer via DC-sputtering.

Results and Discussion

First, we analyzed the solution-ZnO by DSC & TG. This is because it was necessary to decide the proper annealing temperature for the formation of crystal ZnO. As shown in the DSC & TG data in Fig. 1, it was found that ZnO crystallization began at 430 °C [10][11]. Therefore, the samples were heated at 500 °C and 600 °C for 1 hr in air. The XRD pattern (Fig. 2) shows that the ZnO thin films obtained from the spin-coating process have a main peak (002) at 34.4°, demonstrating a crystalline ZnO thin film with a hexagonal wurtzite structure and a preferred orientation having its c-axis perpendicular to the substrate.

Although the ZnO film achieved crystallization at both 500 °C and 600 °C, the low temperature sample had a better thin film property, because of higher intensity in 002. The reason ZnO film with its (002) plane parallel to the substrate is beneficial for device performance is that extrinsic effects such as carrier scattering, which could possibly occur at grain and/or domain boundaries in randomly oriented polycrystalline films, are largely eliminated; sequentially the FET characteristics in a semiconductor channel can be optimal. Also, ZnO 0.05 mol% showed the best characteristics for different concentrations of the precursor solution. After, the ZnO annealed at 500-600 °C for 1 hr.

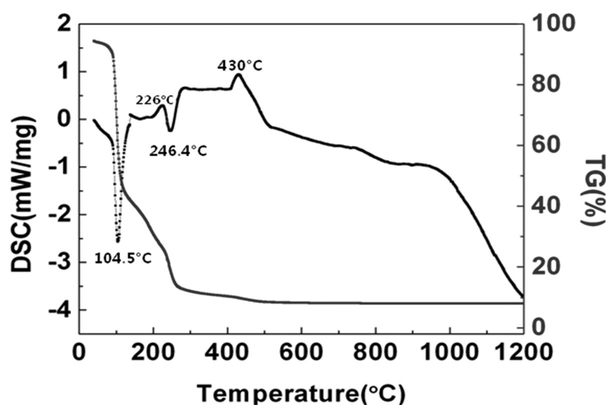

Fig. 1. DTA & TG curves for solution ZnO.

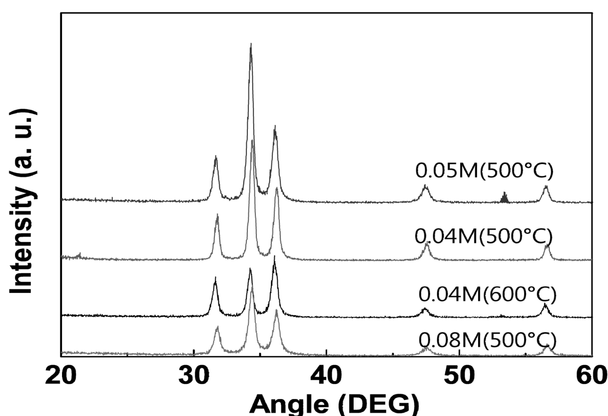

Fig. 2. XRD patterns of ZnO films on Silicon substrate with different concentrations of the precursor solution and annealed 500-600 °C for 1 hr.

The XRD data of the calculated grain size results obtained from X-ray diffraction experiments using the Scherrer formula and calculated from the size of grain (D) is presented next, and calculated as shown in Equation (1).

The equation is expressed as.

$$D = \frac{0.9\lambda}{\beta\cos\theta(rad)} \quad (1)$$

where

D is the mean crystallite dimension, λ is the X-ray wavelength, typically 1.54 Å, β is the line broadening at half the maximum intensity (FWHM) in radians, and is the Bragg angle [12]. Applying the full-width at half-maximum of the peak at $2\theta = 34.4°$ to the Scherrer formula gave an average crystal size of 40 nm for both ZnO crystal films. The FE-SEM images of both ZnO films show that their surface morphology is composed of closely packed particles with a particle size of 30-40 nm (Fig. 3(a), indicating that each particle is a rear ZnO single crystal since this particle size is similar to that calculated from the XRD results. The SEM images of the cross-section of the ZnO film (Fig. 3(b)) indicate that the ZnO thin film and SOG from the spin-coating process have thicknesses of about 100 nm and 800 nm, respectively. Due to Active layer thickness affected performance of semiconductor device, but did not control it in this article. This is because we just attempted to use semiconductor and dielectrode materials in a solution process for a TFT device. Optimal active layer thickness will be determined in a future study.

In terms of TFT device performance factors, the first factor should be the trap states in the semiconductor films (generally arising from grain boundaries) [13]. The second factor should be the contact resistance, caused by the energetic mismatch and interfacial contact between semiconductor and electrode materials [14]. However, a ZnO TFT

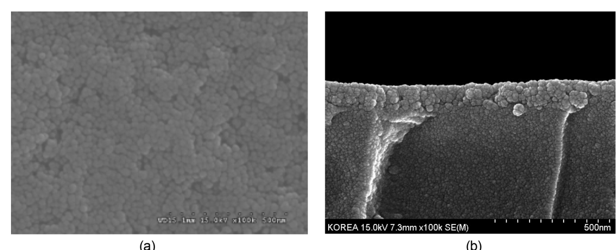

Fig. 3. FE-SEM images of the Zinc Oxide films, (a) Surface, and (b) Cross-section.

fabricated by the spin-coating process already has many trap states and high contact resistance. If a coated layer had high surface energy, up to layer would be difficult to coating using a spin coater. Thus, to achieve a good quality coated layer, it is necessary to reduce the surface energy. In the solution, we treated O_2 plasma in the SOG surface using RIE equipment for reduced surface energy. Fig. 4 show a comparison of the surface energy before and after O_2 plasma treatment. A good quality ZnO layer was achieved after O_2 plasma treatment.

In the last result, Fig. 5(a) displays typical drain current-voltage (I_D-V_D) for a TFT with a ZnO active channel. Under a gate bias (V_G) of 50 V, a saturation current of more than 0.06 μA is achieved with full saturation at a drain bias of 30 V. Fig. 5(b) shows the transfer curves obtained at a drain bias of 10 V. For the ZnO TFT, the estimated saturation mobility is 4.17×10^{-3} cm^2/Vs, V_T is 33 V and I_{ON-OFF} is 2.71×10^3.

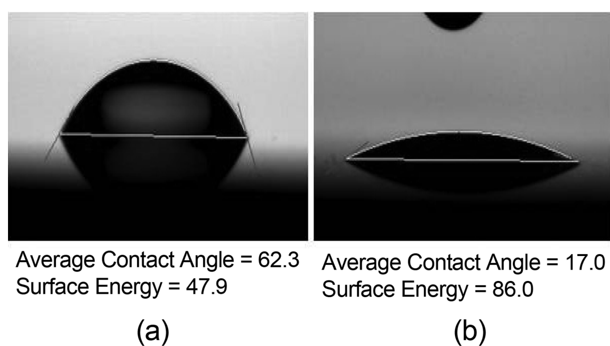

Fig. 4. Contact angle comparisons according to plasma treatment : (a) not treated with O2 plasma, and (b) treated with 02 plasma.

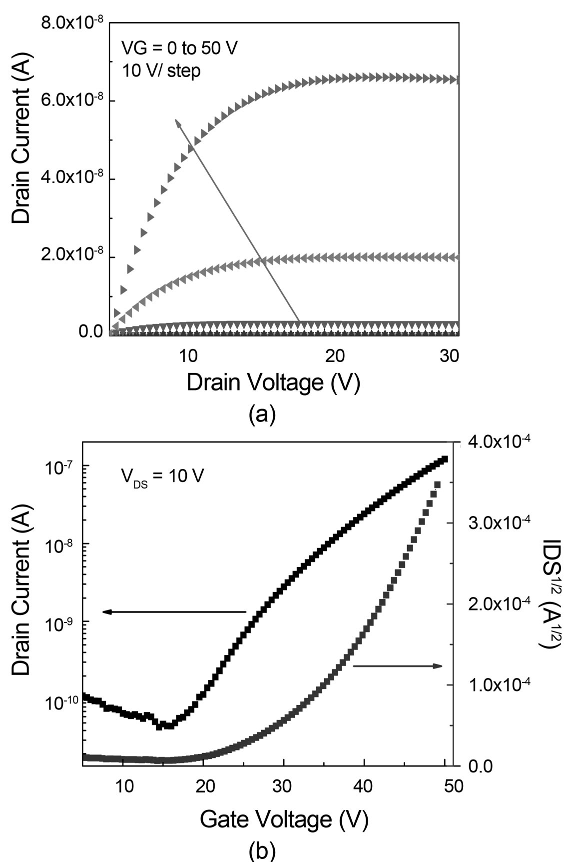

Fig. 5. Electrical properties of ZnO-channel TFT (a) Drain current-drain voltage (ID-VD) output curves, and (b) transfer curves obtained at a drain bias of 10 V.

Conclusion

In this experimental study, ZnO TFTs were fabricated through the solution process. Bottom-gate, top-contact TFTs were constructed on ZnO/SOG/silicon substrate with vacuum deposited thin-film Mo metal as the source/drain electrodes. We predicated annealing condition of ZnO layer as DSC& TG date. The XRD pattern results show ZnO thin films obtained from the spin-coating process have main peak (002) at 34.4°. In addition, the surface of the TFTs was made hydrophilic through O_2 plasma treatment for ease of coating and a good quality ZnO layer. As a result, the estimated saturation mobility is 4.17×10^{-3} cm^2/Vs, V_T is 33 V and I_{ON-OFF} is 2.71×10^3.

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