# Fabrication of diamondlike carbon-coated field emitter triode using aluminum parting layer

Sanjo Lee, Sunup Lee, and D. Jeon[a)]
*Department of Physics, Myong Ji University, Yongin Kyunggi-Do, Seoul 449-728, Korea*

K.-R. Lee, Byeong Kwon Ju, and Myung Hwan Oh
*Korea Institute of Science and Technology, P.O. Box 131, Cheongryang, Seoul 130-010, Korea*

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Coating silicon field emitter tips with a thin film of diamondlike carbon (DLC) seems to be a promising way to improve the performance of the silicon emitter tips. If one deposits a DLC film directly onto the gated silicon emitter, DLC will contaminate the side wall of the insulating layer, which can cause a large leakage current to the gate. To prevent the contamination of the side wall, we deposited an aluminum sacrificial layer before coating the DLC film. The gate current measured from the DLC-coated emitters using the sacrificial layer was less than 3% of the anode current. © *1998 American Vacuum Society*. [S0734-211X(98)13503-5]

## I. INTRODUCTION

Silicon field emitter devices are becoming popular because of the reproducible and reliable fabrication process based on the silicon very large scale integrate (VLSI) technology.[1] Nevertheless, most of the prototype field emission displays announced so far adopted metal tips. The lower electrical conductivity of silicon does not seem to be a reason for this because the current requirement for field emission displays is very small. More significant reasons perhaps are that silicon is fragile against ion sputtering damage and that silicon exhibits low thermal conductivity, which are the important factors in determining the lifetime of field emitter devices. To avoid the handicap of silicon emitters, an effort such as coating silicon emitters with a thin film of metal, silicide, diamond, or diamondlike carbon (DLC) has been tested. In this report, we present the result of coating DLC on a gated silicon field emitter. We first deposited a DLC film using chemical vapor deposition (CVD) method directly onto the gated silicon emitter tips. Although the emission current fluctuation was improved after the DLC coating, we found that the leakage current to the gate increased.[2] This was because the CVD DLC film not only coated the silicon tips but also contaminated the side wall of the insulating layer. The contaminated surface supplied a current path from the substrate to the gate, and thus the leakage current increased. To avoid the contamination problem, we protected the side wall with an aluminum sacrificial layer before DLC deposition. With this additional process, we could reduce the gate current to less than 3% of the anode current.

## II. EXPERIMENT

The process of our DLC coating is shown in Fig. 1. First, using an $n$-type silicon wafer, emitter tips were formed under the oxide masks by dry etching. The tip was then sharpened by oxidation of the surface. An insulating layer and a gate film were deposited by electron beam evaporation. After this usual process for fabricating silicon triode, we deposited aluminum, while rotating the substrate, from vicinal angle using electron beam evaporation so that an aluminum film was formed on the side wall of the insulating layer. To expose the tip, the oxide cap and the oxide layer on the tip surface were removed by wet etching. Before DLC coating, the gated silicon tips were cleaned by $Ar^+$ ion bombarding for 1 min. The ion beam voltage was 400 V. DLC was coated using $Ar^+$ ion sputtering of a high purity carbon target. In this method, $Ar^+$ ions sputter a carbon target and carbon clusters desorbed from the target adhere to the substrate and form a DLC film. The properties of DLC grown by this method are similar to those of laser ablation-grown DLC, i.e., it is free of hydrogen and contains high density $sp^2$ bonding.[3] The deposition was done for 30 min. It is difficult to measure the exact thickness of the DLC at the apex of the tip. On a flat substrate, the DLC film deposited using the same condition became 300 Å thick after 30 min. Since the film is very thin, we think the DLC film coats the substrate rather uniformly. However, coating with a thick DLC film resulted in the decreased aspect ratio of the emitter tip.[4] The device was completed by removing the aluminum parting layer. The $I-V$ data were measured under the vacuum pressure of $10^{-7}$ Torr. The device used for $I-V$ measurement contained 3600 emitter tips in the area of $300\times300$ $\mu$m$^2$.

## III. RESULTS AND DISCUSSION

The top view of the completed device is shown in Fig. 2. The gate hole diameter is 1.5 $\mu$m and the distance between the holes is 5 $\mu$m. Points at the center of the holes are the apex of the DLC-coated tips. To measure the $I-V$ data, the cathode tips were grounded and the extraction voltages were applied to the gate. The anode was placed 1 mm above the gate and was applied with 300 V. In Fig. 3, we show $I-V$ curves obtained from the DLC-coated silicon emitters. The curve marked with triangles was obtained from the emitter coated with CVD–DLC without using the aluminum sacrificial layer and the other curve marked with circles from the

[a)]Corresponding author; electronic mail:jeon@wh.myongji.ac.kr

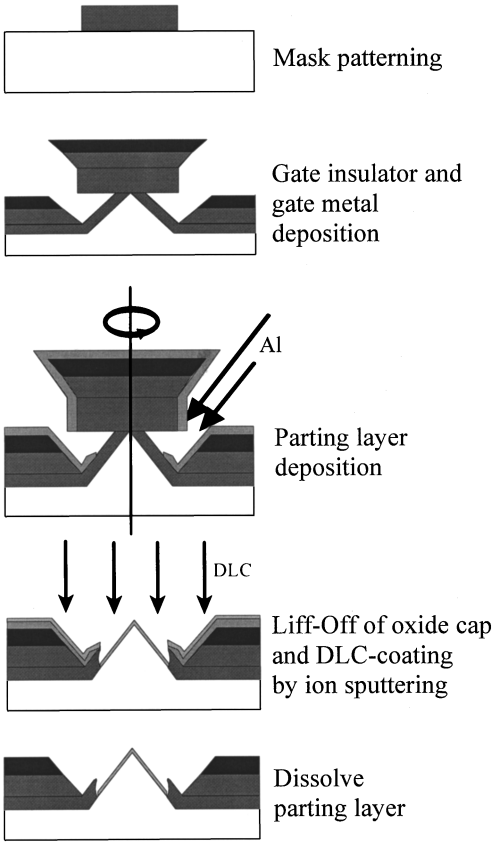


FIG. 1. Fabrication process of the DLC-coated silicon tips with extraction gate holes.

emitter coated with the sputter-grown DLC using the sacrificial layer. (Silicon tips fabricated from the same wafer were used for both sample preparation.) The data show that the anode currents from both samples are almost the same, but the gate current for the latter is smaller by a factor of 10. Current can leak to the gate due to the emission through vacuum or via contaminated surface. Since the CVD coating can cover the stepped surface uniformly, the side wall of the insulating layer can be contaminated during DLC coating of the tips. We reckon that this is one of the reasons for the

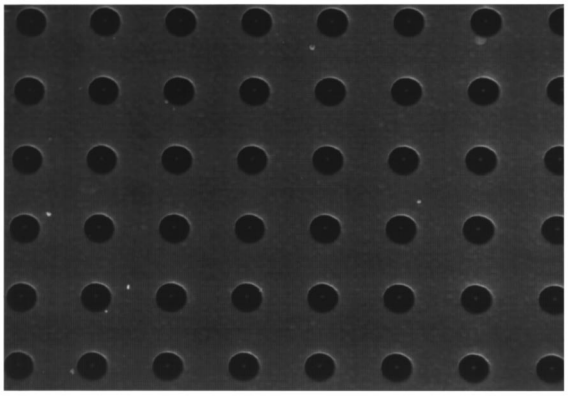

FIG. 2. Scanning electron micrograph of the DLC-coated silicon tips with extraction gate holes.

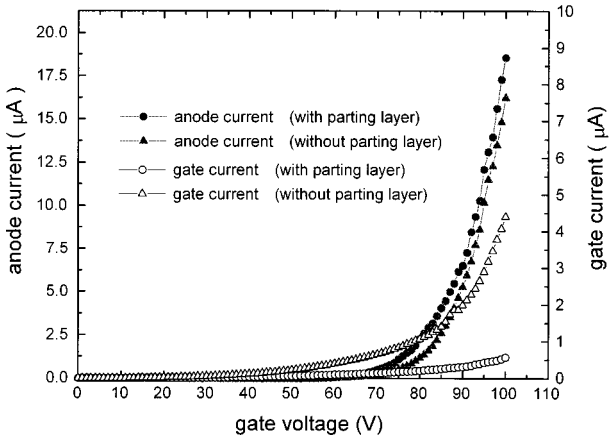


FIG. 3. $I-V$ curves of the DLC-coated silicon tips. Tips coated with DLC using aluminum parting layer exhibits smaller gate current.

larger gate current for the tips coated with DLC without Al cover. At low voltage, the gate current is larger than the anode current for the tips coated with DLC without Al cover. In Fig. 4, we plot the corresponding Fowler–Nordheim (F–N) curves of the anode and gate $I-V$ data shown in Fig.

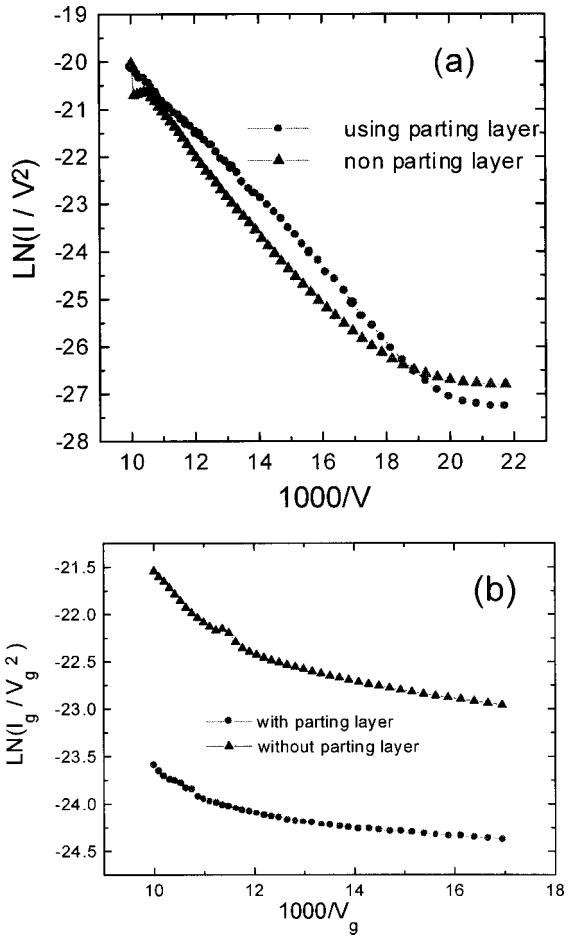


FIG. 4. Fowler-Nordheim curves of the corresponding $I-V$ data shown in Fig. 3. (a) Anode current, (b) gate current.

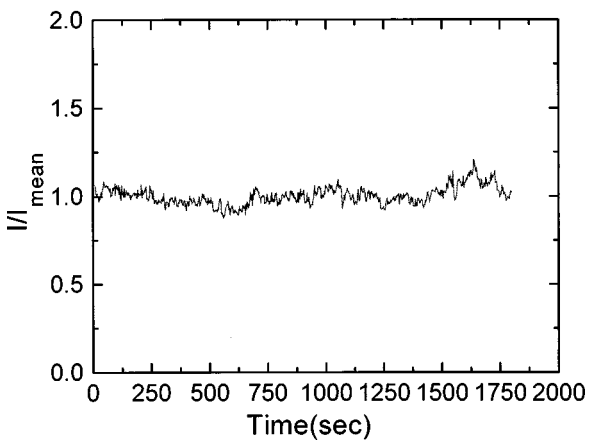


FIG. 5. Short term fluctuation of the anode current from the DLC-coated silicon tips.

3. The F–N curves for the anode current are a typical emission curve, but the slope of the gate F–N curves is gentle and bends at high voltages.

We also measured the short term fluctuation of the anode current from the DLC-coated silicon tips, of which the result is plotted in Fig. 5. A well-known technique to reduce the current fluctuation from the metal tips is to insert a resistive layer in series with the emitter. Although the effect or the role of coating layer over the silicon or metal tips is uncertain at the moment,[5] if there is a voltage drop across the DLC coating layer, the same effect of current stabilization is expected. This effect was in fact demonstrated using DLC-coated Mo tips.[6] If the coating layer is too thick, the voltage drop across the coating layer will be large and the tip apex will become dull. In this case, the tip may be very well protected but the emission will become poor. Actually, the emission current presented in Fig. 3 was reduced by about one fifth the current we achieved from the same silicon tips before coating. It has been reported that DLC coating of tips could increase the emission current.[6] However, the mechanism of electron emission from DLC or diamond is not yet understood. There is a suggestion that the work function of these materials is low, but this is inclusive because the work function calculated from Fowler–Nordheim curves reflects the geometrical effect as well as the material properties. The emission from flat DLC films does show dependence on the film thickness, and the trend is that the emission decreases as the film gets thicker. We think that this is the case for our DLC coating of silicon tips. Therefore, it will be interesting to study the optimum thickness of the coating layer to achieve both the current stabilization and the tip protection. In Fig. 6, we show the emission patterns of our DLC-coated silicon tips. The phosphor screen started to glow at the gate voltage of 76 V.

## IV. CONCLUSION

The performance of silicon field emitter tips can be improved by coating the tips with DLC. However, if DLC contaminates the side wall of the insulating layer during the coating process, there will be a large leakage current to the gate through the contaminated surface. To avoid the contamination, we used an aluminum sacrificial layer to protect the side wall. As a result, the leakage current to the gate after DLC coating was reduced by a factor of 10. Because of the possible voltage drop across the DLC coating layer, the emission current was reduced compared to the uncoated tips, but the short term current fluctuation was improved.

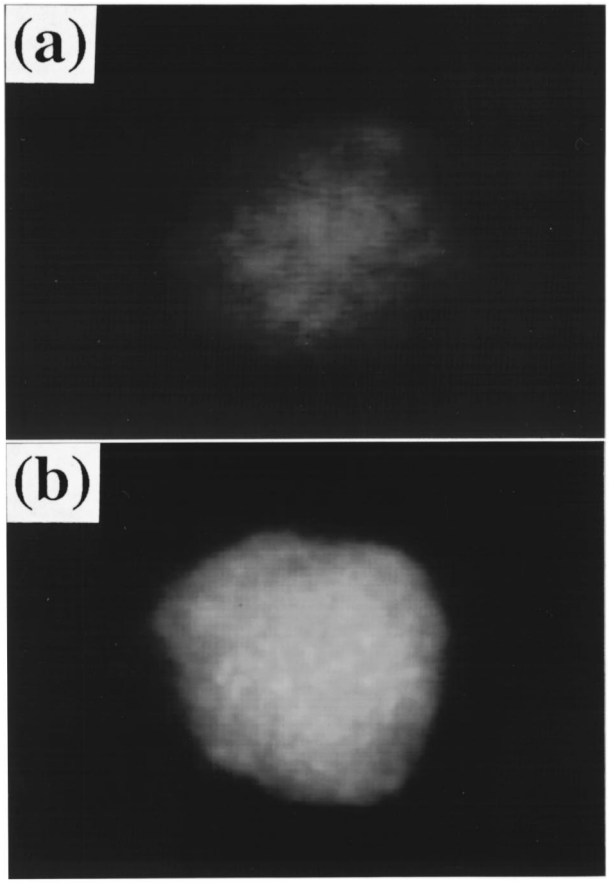


FIG. 6. Emission patterns at different gate voltages. The screen voltage was 300 V and was placed 1 mm above the gate. The gate voltage was 76 V and the anode current was 1.2 $\mu$A for the dim pattern (a) and 100 V and 19 $\mu$A for the bright pattern (b), respectively.

## ACKNOWLEDGMENTS

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