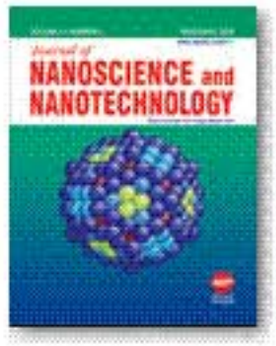
Post Annealing Effects on the Electrical Characteristics of Pentacene Thin Film Transistors on Flexible Substrates



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Post Annealing Effects on the Electrical Characteristics of Pentacene Thin Film Transistors on Flexible Substrates

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This work studies the effect of post annealing of pentacene on a flexible substrate through the examination of electrical properties and surface morphologies. It is confirmed that the best performance of devices is achieved when the post annealing temperature is 60 °C, since the grain size increases, which decrease grain boundaries caused charge transport limit. We can also confirmed the large threshold voltage shift of device annealed at 60 °C that means the lower trap density between channel and insulator interface. The device annealed at 60 °C exhibits a saturation mobility of 1.99 $cm^2/V \cdot s$, an on/off ratio of 1.87×10^4, and a subthreshold slope of 2.5 V/decade.

Keywords: Post Annealing Effect, Poly-4-Vinylphenol, Polyethylene Naphthalate, Organic Thin Film Transistor.

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1. INTRODUCTION

Organic thin film transistors (OTFTs) have received much attention due to their great potential for use in flexible electronics applications, including electronic paper, radio frequency identification (RFID) tags, smart cards, and flexible displays.[1–4] Among all the organic semiconductors used to fabricate OTFTs as active materials, pentacene is the most commonly used because of its remarkable carrier mobility.[5] The performance of OTFTs using pentacene is related to grain growth, crystalline ordering, and the resulting defects. Among the methods available for increasing the grain size and removing the defects, the post annealing method is the most appropriate for easily improving the performance of organic devices.[6] For this reason, there have been several studies of the annealing effects of OTFTs based on rigid substrates, such as a Si substrate.[7–8] Fukuda et al. examined the effects of annealing on OTFTs using polyimide gate dielectric layers.[9] However, from all the research studies, it has been found that the annealing temperatures for pentacene and the gate dielectrics are all quite different. Therefore, it is important to find the optimum annealing temperature according to the gate dielectrics but there are no sufficient studies, to date, on these annealing effects based on flexible substrates with organic gate dielectrics, such as poly-4-vinylphenol (PVP). Dielectrics made of organic materials show a high compatibility with plastic substrates and to apply pentacene for devices based on plastic substrates with organic dielectrics, it is necessary to investigate its thermal annealing effects, as well as analyzing the growth of the pentacene and the molecular ordering. In this study, bottom-gate and top-contact pentacene TFTs with spin coated PVP dielectric layers are fabricated on a polyethylene naphthalate (PEN) substrate. Then the optimum post annealing temperature is confirmed for the flexible OTFTs.

2. EXPERIMENTAL DETAILS

Figure 1 shows the structure of a top-contact OTFT on a PEN substrate. A 150 nm thick indum-tin oxide (ITO, sheet resistance $\sim$10.0 ohm/γ) is deposited on a 100 μm thick PEN substrate by RF-sputtering. A cross-linked PVP film is used as the gate dielectric and to make the PVP solution, the PVP (Sigma-Aldrich, $Mw \sim 20000$) is mixed with 10 wt% of propylene glycol monomethyl ether acetate (PGMEA), then a poly melamine-co-formaldehyde methylated (Sigma-Aldrich, $Mw \sim 511$) is added, which serves as a cross-linking agent to the PVP solution in a 1:10 ratio. After the PVP solution is formed, the PVP dielectric layer is spin coated on the PEN substrate with the ITO, then

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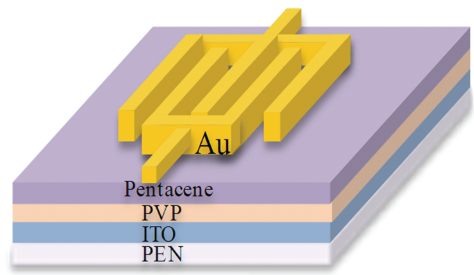

Fig. 1. Schematic view of pentacene thin film transistors with interdigitated-finger-type electrodes. The pentacene TFTs have been annealed for 2 h.

cross-linked at 200 °C for 10 mins on a hot plate. The 300 nm thick PVP dielectric layer is formed. A 70 nm-thick pentacene (Sigma-Aldrich) layer is deposited at a rate of 0.3 Å/s by using a thermal evaporator (DOV Co., Ltd.) under a pressure of 1×10^{-6} Torr. A 200 nm-thick Au electrode is deposited through a shadow mask by using the thermal evaporator using a interdigitated-finger geometry for the electrodes, which enhances the saturation mobility and reduces the total resistance of the transistors.[10] The channel length (L) and width (W) are 100 μm and 2500 μm, respectively. After the deposition of the Au electrode, each device is annealed in an oven with N_2 environment for 2 h at 40 °C, 60 °C, 80 °C, and 100 °C, respectively. The surface morphology and crystallinity of the pentacene films are investigated by using AFM and XRD spectroscopy in the symmetric reflection coupled arrangement, with a Cu Kα_1 radiation ($\lambda_{K\alpha 1} = 1.54$ Å) X-ray source. Electrical characteristics of the proposed devices are measured by a semiconductor characterization system (Keithley SCS 4200) in a dark box.

3. RESULTS AND DISCUSSION

Figure 2 shows the XRD spectra of the pentacene films where all of these appear as a series of patterns with (0 0 1) peaks. High intensities can be seen at $5.64 \pm 0.04°$ in 2θ, corresponding to an inter-layer spacing (d) of 15.6 ± 0.1 Å, which is similar to the thin film phase of the pentacene film,[11] where the c axis of a molecule is located perpendicular to the dielectric. The inter-layer spacing (d) value is obtained by Bragg's equation, as follows:

$$d = \frac{\lambda_{K\alpha 1}}{2\sin\theta} \quad (1)$$

where θ is a half of the measured degree, and $\lambda_{K\alpha 1} = 1.54$ Å, which is the wavelength of the Cu $K_{\alpha 1}$ X-ray source. Post annealing improves the XRD intensity as shown in Figure 2, and after annealing at 60 °C, the intensity of the (0 0 1) peak is higher than the one of pentacene annealed at other temperatures. These high peak intensities indicate a well-ordered pentacene molecular structure.[12] The XRD intensity of (0 0 4) Bragg's peak is not observed, when the post annealing temperature is 100 °C. This dramatic decrease of intensity indicates thermal disorder, and an uncorrelated lattice disorder.[13] The inset is the magnified of the (0 0 1) peak which shows the full width at half maximum (FWHM). The reduction in FWHM at 60 °C annealing temperature implies that the grain size of pentacene is increased after post annealing. Figure 3(a) shows a 3 μm × 3 μm AFM image of non-annealed 70 nm-thick pentacene film and Figures 3(b)–(e) show the morphologies of the pentacene films after post annealing treatments at 40 °C, 60 °C, 80 °C, and 100 °C. Figure 3(f) shows the effect of post annealing on grain area and the root mean square (RMS) roughness. The RMS roughness is increased with increasing the thermal annealing temperature. The grain area of the pentacene film increases as the post annealing temperature increases to 60 °C as shown in Figure 3(f). However, it decreases slightly as the temperature continues to increase, which represents an increased portion of the grain boundaries. These may be due to a weak intermolecular van der Waals force of the pentacene film.[14] The AFM image of device annealed at 100 °C shows grains with rough surfaces and undefined edges. It is believed that grains of pentacene film are damaged because of such high temperatures, since the organic semiconductor are bonded by the weak van der waals force,[15] thus in high temperature their bonding can be broken easily. Figure 4 shows typical p-channel characteristics of the output characteristic of the proposed OTFTs. The drain current increases linearly at a low drain voltage, then saturates with an increasing drain voltage. There is no resulting S shape in the early part of the output curve, as shown in Figure 4, which means a low potential barrier between the pentacene and the Au electrode indicating a good ohmic contact between two layers. The device annealed at 60 °C shows a much higher drain current than thenon-annealed device. This phenomena is caused by easy charge transport of the device annealed at 60 °C from source to drain

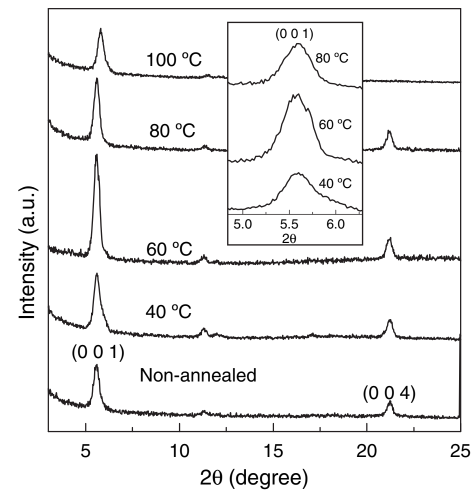

Fig. 2. XRD spectra on the pentacene films annealed at various temperature. The inset is the magnified of the (001) plane.

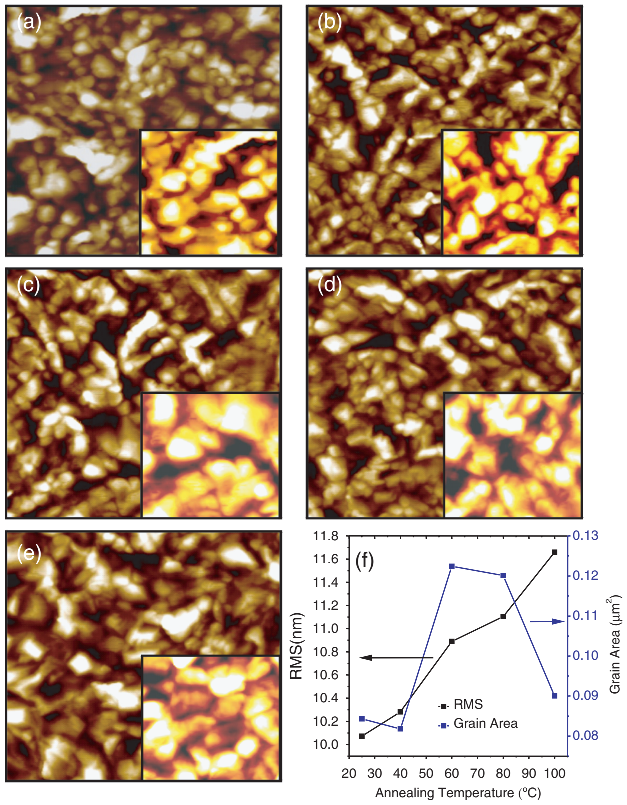

Fig. 3. 3 μm × 3 μm AFM images of pentacene films on PVP dielectrics based on PEN substrate: (a) non-annealed, (b)–(e) after annealing at 40 °C, 60 °C, 80 °C, and 100 °C. (f) The effect of thermal annealing on RMS roughness and grain area. The insets are 1 μm × 1 μm AFM images of pentacene film.

because of decreased grain boundaries. The characteristics of the devices can be obtained from the transfer curves, as shown in Figure 5. The saturation mobility (μ_{sat}) of the OTFT can be extracted from the following equation,[16]

$$I_D = \frac{WC_i}{2L}\mu_{sat}(V_G - V_{th})^2 \tag{2}$$

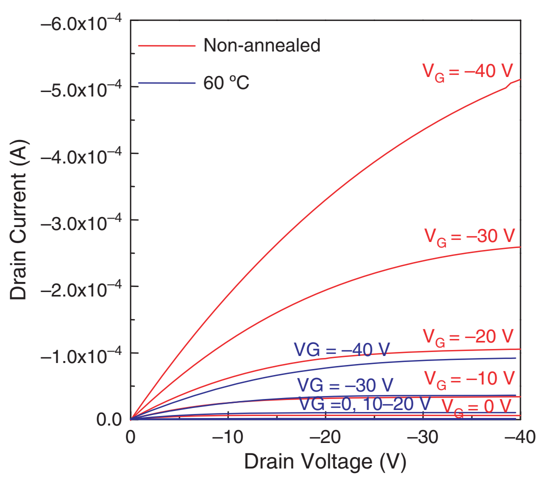

Fig. 4. The output characteristics of flexible pentacene TFTs with PVP gate insulators without and with post annealing at 60 °C.

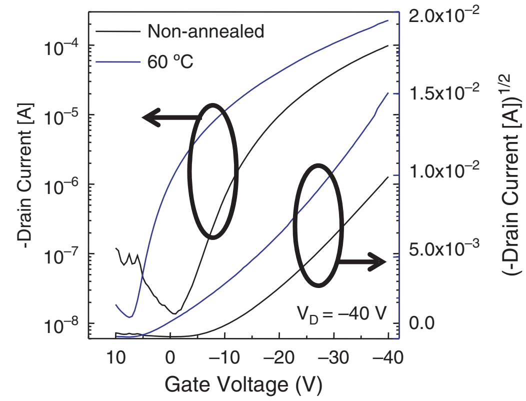

Fig. 5. Transfer characteristics of flexible pentacene TFTs with PVP gate insulators without and with post annealing at 60 °C.

where I_D is the drain–source current, L is the channel length, W is the width of the channel, C_i is the capacitance per unit area of the dielectric. V_G is the gate voltage, and V_{th} is the threshold voltage. The drain current is defined at $V_G = -40$ V and $V_D = -40$ V. Figure 5 shows that the V_{th} of OTFT annealed at 60 °C appears lower than the one without annealing. Since V_{th} is related to the interfacial trap density at the active channel/gate insulator interface if the entire active layer contains the same amount of deep level defects,[17] the OTFT annealed at 60 °C contains less positive trap density than the non-annealed OTFT at the pentacene/PVP dielectric interface.[18] Table I shows a summary of the electrical parameters, with variations in the post annealing temperature. As seen in Table I, the mobility increases from 0.99 to 1.99 cm²/V·s until the annealing temperature reaches 60 °C, then it decreases from 1.99 to 0.52 cm²/V·s as the annealing temperature increases above 60 °C. The mobility and on/off ratio of the OTFTs annealed at 60 °C is the highest, and the sub-threshold swing is lowest at 60 °C. From these results, it is verified that the proposed device, annealed at 60 °C, shows good performance. And it can be seen that post-annealing at temperatures above 60 °C results in the degradation of the mobility, and the on/off ratio. These results indicate that annealing at above 60 °C leads to the grain size reducing and crystallinity mis-orienting. Carlo et al. examined the field-effect mobility and found that it is strongly related to the grain size.[18] The mobility declines as the grain size

Table I. Summary: The electrical characteristics of OTFTs at various post annealing temperatures.

Annealing temperature (°C)	Parameters			
	μ_{sat} (cm²/V·s)	I_{on}/I_{off}	$S.S$ (V/decade)	V_{th} (V)
Non-annealed	0.99	7.22×10^3	4.3	−12
40	1.43	9.89×10^3	3.9	−9
60	1.99	1.87×10^4	2.5	−7.5
80	1.41	1.19×10^4	3.2	−9
100	0.52	1.14×10^4	3.6	−10

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decreases, because many grain boundaries limit the charge transport in the organic film.[19] The increase of subthreshold slope is due to recharge of incomplete ionized acceptors or traps at interface or in the bulk.[20] A reduction of subthreshold slope of devices annealed at 60 °C indicates that post annealing reduces incomplete ionized acceptors and traps. That is a good interface is formed between pentacene and the PVP dielectric.

The electrical properties of devices annealed at various temperatures are coincident with the AFM and XRD results, so it is concluded that the selection of post annealing temperature is important to improve the performance for flexible pentacene TFTs with PVP.

4. CONCLUSION

In summary, the post annealing effects of pentacene TFTs, based on a PEN substrate with the PVP dielectric, have been examined. Post annealing results show grain growth along the *c* axis, and an improvement in mobility. When the post annealing temperature is 60 °C, the performance of the device is at its best and this is shown from the AFM and XRD results. However, annealing with a temperature $>$ 60 °C decreases the electrical properties, such as the mobility and the on/off ratio, and devices annealed at temperatures above 80 °C exhibit a dramatic decrease of performance because of the subsequent decrease of grain size, mis-oriented crystallization and damage of the grains. It is clear that the low XRD peak intensity of an annealing temperature of 100 °C, and the grain size shown AFM image is slightly decreased. It has been confirmed from this study that the optimum post annealing temperature for fabricating OTFT based on PEN substrate with PVP dielectrics is 60 °C.

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