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Pulsed DC Bias Effects on *p*-Type Semiconductor $SrCu_2O_2$ Film Deposited by RF Magnetron Sputtering

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Transparent *p*-type semiconducting $SrCu_2O_2$ films have been deposited by RF magnetron sputtering under unbalanced bipolar pulsed DC bias on low-alkali glass substrates in a mixed gas of 1% H_2/Ar below 400 °C. The pulsed DC bias voltages to substrate were varied from 0 V to −200 V with a frequency of 350 kHz. The effect of pulsed DC bias on the structure and electrical and optical properties of $SrCu_2O_2$ films has been investigated using SEM, XRD, surface profiler, Hall measurements and UV-VIS spectrometer. The deposition rates of $SrCu_2O_2$ films under DC-pulsed bias show a maximum at −100 V bias, and decreased with increasing the bias voltage. XRD results of the as-deposited films under the bias voltage at 400 °C reveal $SrCu_2O_2$ polycrystalline phase, and increased crystallite size with increasing pulsed DC bias voltage. The $SrCu_2O_2$ films deposited under the pulsed-bias of −100 V exhibits the highest conductivity of 0.08 S/cm, and over 70% of transmittance at 550 nm. It is confirmed that the application of pulsed DC bias in sputtering improves the crystallization, crystal growth, and the electrical and optical properties eventually under 400 °C.

Keywords: *p*-Type Semiconductor, $SrCu_2O_2$, RF Sputtering, Unbalanced Bipolar Pulsed DC Bias.

RESEARCH ARTICLE

1. INTRODUCTION

Transparent electronics is an emerging technology that employs wide band-gap semiconductors, which have a band gap energy more than about 3.2 eV.[1] In order to realize the invisible electronic circuits, transparent active components such as transparent diodes, TFTs, and CMOSs, etc., including transparent electrodes, should be developed. Oxide semiconductors are very promising materials because they can satisfy simultaneously high/low conductivity with high visual transparency in the visible light range of 400 nm∼800 nm. Transparent oxide semiconductor based transistors have recently been proposed using as active channel intrinsic ZnO.[2] TCOs such as Sn-doped In_2O_3 (ITO), *F*-doped SnO_2 (FTO) are widely used as transparent electrodes for LCDs, touch panels, solar cells, and organic light emitting diodes (OLEDs) etc.[3–5] But most TCOs exhibits *n*-type electrical conductivity, thus there are little applications based on the transparent *p*–*n* junctions due to the lack of *p*-type TCOs.

Since first report on $CuAlO_2$[6] by Hosono et al. various *p*-type TCOs, which have delafossite structure such as $CuGaO_2$[7] etc. have been reported.

According to Kudo et al.[8] $SrCu_2O_2$, which is non-delafossite *p*-type semiconductor, can be deposited by PLD (pulsed laser deposition) onto glass substrates at 300 °C, and Bobeico et al.[9] have been reported $SrCu_2O_2$ films by *e*-beam evaporation technique at 350 °C with transparency of about 60%. and $SrCu_2O_2$ films deposited by RF magnetron sputtering at 500 °C have been reported by our group.[10]

In the viewpoint of commercial applications, lower substrate temperature gives important advantages such as flexible choice of substrate materials and lowering process temperature etc. Recently, bias sputtering process has attracted much attention because it is beneficial to the crystallization and grain growth of oxide thin films at relatively lower deposition temperature.[11–13] Pulsing the substrate bias voltage in the mid-frequency (100∼350 kHz) region increase the ion current near the substrate, and this phenomenon offers an additional means of controlling the ion current.[14]

In this study, in order to seek lowering crystallization temperature of typical *p*-type semiconducting $SrCu_2O_2$,

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the effect of pulsed DC bias voltage on the structure and electrical and optical properties of $SrCu_2O_2$ films has been investigated.

2. EXPERIMENTAL DETAILS

2.1. $SrCu_2O_2$ Thin Films Fabrication

Single-phase $SrCu_2O_2$ powder has been synthesized by 2-step solid state reaction at 950 °C under N_2 atmosphere. In this study, unbalanced bipolar pulsed DC bias with the frequency of 350 kHz was applied during the RF magnetron sputtering. Generally, the on-time of the applied pulse means the portion of a pulsing period with a negative voltage. In our experiment, the reverse time (the time of the positive-pulsing period) of the applied pulse was fixed to 1.1 μs, and duty factor, which is defined as the on-time ratio to the complete pulse period, was 61.5%. The transparent *p*-type semiconductor $SrCu_2O_2$ films were deposited on 20 mm × 20 mm-sized low alkali glass (eagle 2000, Corning, USA) by RF magnetron sputter (LSS-01, J&L Tech, Korea). Substrates were washed with acetone, methanol for 15 minutes and rinsed in D.I water. The base pressure in the chamber prior to deposition was better than 9×10^{-4} Pa and fabricated $SrCu_2O_2$ target was pre-sputtered for 10 minutes. Power of $SrCu_2O_2$ sputtering has been 2 W/cm^2 in 1% H_2/Ar mixed gas atmosphere. From the preliminary experimental results, the target-substrate distance was fixed in 70 mm. Working pressure in the chamber has been 2.6 Pa during deposited 90 minutes. Substrate temperature was maintained as 200 °C, 300 °C, and 400 °C. The pulsed DC bias voltages to substrate were varied from negative 0 V to −200 V with the interval of 50 V. The detailed synthetic procedures for $SrCu_2O_2$ powder, targets, and thin films were reported previously.[10]

2.2. Characterization of $SrCu_2O_2$ Thin Films

In these symposiums, stimulating lectures and presentations by distinguished speakers from all over the world are planned for the ICAE 2011. In addition to the professional exchange of ideas, it will be a place to meet friends who share common research objectives and to have chances for further co-work that may result in mutual achievements. Thickness and deposition rates of $SrCu_2O_2$ thin films were measured with a surface profiler (Alpha step 500, Tencor, USA). Crystalline phases of the films were confirmed using X-ray diffraction (Rigaku D MAX2200, Japan, Cu $K\alpha$, 40 kV/30 mA). Optical transmittance spectra of the films were measured in the wavelength range from 200 to 1200 nm with a *UV-VIS* spectro-photometer (V-570, JASCO, Japan). The surface morphology of $SrCu_2O_2$ thin films was observed using scanning electron microscope (JSM-6380, JEOL, Japan). Electrical properties, such as electrical mobility, carrier concentration and electrical conductivity, of each films were measured by Hall measurement system (HMS-3000, ECOPIA, Korea) using a van der Pauw method.

3. RESULTS AND DISCUSSION

Figure 1 shows the XRD spectra for the $SrCu_2O_2$ thin films deposited at 400 °C with different pulsed DC bias voltages. One can see the crystal phase of the deposited film without bias is amorphous, as our group reported previously,[10] and $SrCu_2O_2$ polycrystalline phase with −50 V to −100 V bias, and metal Cu phase above −150 V bias. Figure 1 reveals the pulsed DC bias on the substrate improves the crystallinity of the deposited films. A negative bias applied to the substrates attracts positive ion components in the plasma state, and results in the bombardment to the surface of the depositing films.

Figure 2 shows the proportional relationship between the substrate pulsed DC bias voltage to the bias (ion) current, which is induced by the plasma, at a constant pulse frequency of 350 kHz; the increased bias voltage results in the increased bias (ion) current. So, similar to sputtering, the re-emission is caused by ion bombardment of the deposited material. This is the reason why Cu phase resulted above −150 V bias. Wang et al.[15] reported that the variation in the stoichiometric ratio of Co/Sm of $SmCo_5$ films with the substrate bias was attributed to re-sputtering of Co atoms from the growing films due to the mass effect. From the same reason, Cu atoms are thought to re-sputtered preferentially compared to more heavy Sr atoms from the surface of the $SrCu_2O_2$ films, and re-deposition occurs as the metallic Cu phase. This is plausible reason when we consider the defect formation energies in $SrCu_2O_2$; 1.29 eV for Cu vacancy, and 5.50 eV for Sr vacancy for *p*-type (oxygen excess) defects.[16] The crystallite size of the $SrCu_2O_2$ films evaluated from the Scherrer

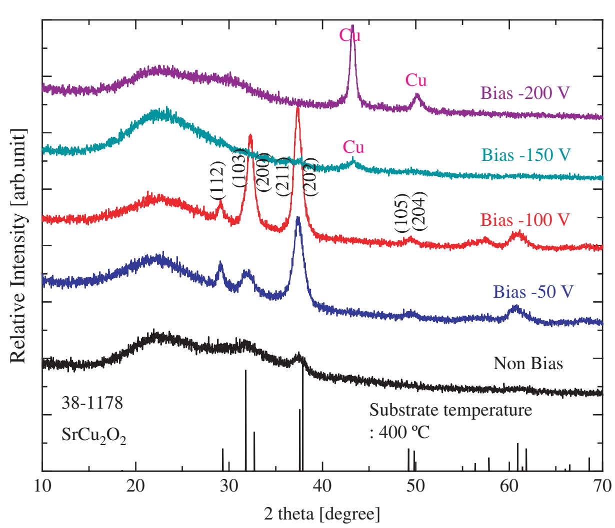

Fig. 1. X-ray diffraction patterns of $SrCu_2O_2$ thin films deposited at 400 °C.

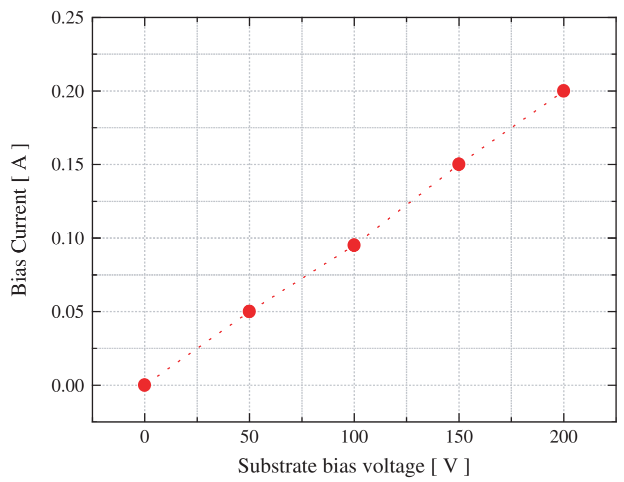

Fig. 2. Relationship between the substrate pulsed DC bias voltage and bias current. (Substrate temp.: 400 °C, pulse frequency: 350 kHz.)

formula increase with increasing the bias voltages; about 25 nm, 40 nm, 60 nm for 0V, −50 V, and −100 V, respectively.

In Table I, the crystal phase of the $SrCu_2O_2$ thin film at various deposition conditions was summarized. It is noteworthy that the deposition without pulsed DC bias results in amorphous phase in all the experimental condition in this study, and $SrCu_2O_2$ phase appears only above 500 °C,[10] but the crystalline $SrCu_2O_2$ phase results with pulsed DC frequency from 300 °C with the application of the 350 kHz-pulsed DC bias.

Figure 3 shows the deposition rate of $SrCu_2O_2$ thin films. The deposition rates of $SrCu_2O_2$ films under pulsed DC bias show maxima at −100 V bias in the substrate temperature of 200 °C to 400 °C. The deposition rates of the $SrCu_2O_2$ thin films are increased up to −100 bias voltage, and then decrease above −100 V. This is similar to the results of ZnO:Al by Ma et al.[17] and can be explained by re-sputtering from the surface of the deposited films. It is thought that the increasing in the Cu re-sputtering rate according the bias voltage results in the decrease in the deposition rate.

Figure 4 shows the transmittance of the $SrCu_2O_2$ thin films at various pulsed DC bias voltages at the substrate temperature of 400 °C. The film thicknesses are 200 nm, 310 nm, and 350 nm at 0 V, −50 V, and −100 V,

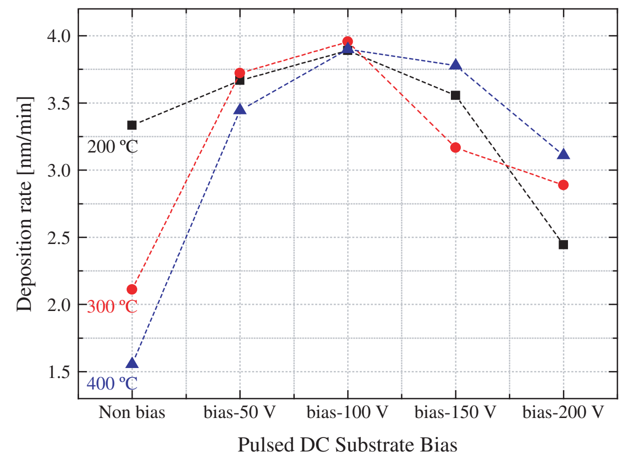

Fig. 3. Deposition speed of $SrCu_2O_2$ thin films.

respectively. The transmittance of the film increases with increasing pulsed-DC bias voltages. It is thought that the increased crystallinity results in the increased transmittance, as was analyzed from the full-width at half maximum (FWHM) of XRD results. The optical band gap deduced from the transmittance measurements shows 3.29 eV, which is similar to our previous report.[10]

Table I shows the summary of the transmittance crystal phase of $SrCu_2O_2$ thin film at various deposition conditions. The transmittance of the film deposited at 300 °C and −100 V bias, and 400 °C and −100 V bias reveals 57%, 70%, respectively. The improved transmittance of the $SrCu_2O_2$ thin film deposited at 400 °C is resulted from the increased crystallinity and crystallite size, as was seen from XRD, SEM results.

Figure 5 shows SEM images of $SrCu_2O_2$ films deposited at 400 °C with and without bias voltages. The SEM images reveals that the crystallite size with −100 V bias is increased compared to that of 0 V bias. It is thought that the bombardment owing to the negative bias to the substrate gives an additional energy to the cationic components to move on the surface of the substrate, as is the case in the higher temperature, and results in increasing the crystallite size.

Figure 6 shows the electrical properties of $SrCu_2O_2$ thin film deposited at 400 °C under the various substrate bias voltages. Even though the correct values of the carrier concentration in this study are somewhat obvious because of

Table I. Summary of the crystal phase and the transmittance of the $SrCu_2O_2$ thin film at various deposition conditions.

	200 °C		300 °C		400 °C	
	Crystal phase	Transmittance [@550 nm, %]	Crystal phase	Transmittance [@550 nm, %]	Crystal phase	Transmittance [@550 nm, %]
Non-bias	Amorphous	5	Amorphous	16	Amorphous	55
−50 V bias	Amorphous	59	$SrCu_2O_2$ $SrCu_2O_3$	61	$SrCu_2O_2$	66
−100 V bias	Cu_2O	44	$SrCu_2O_2$	57	$SrCu_2O_2$	70
−150 V bias	Amorphous	50	Cu	37	Cu	27
−200 V bias	Amorphous	66	Cu	18	Cu	0.5

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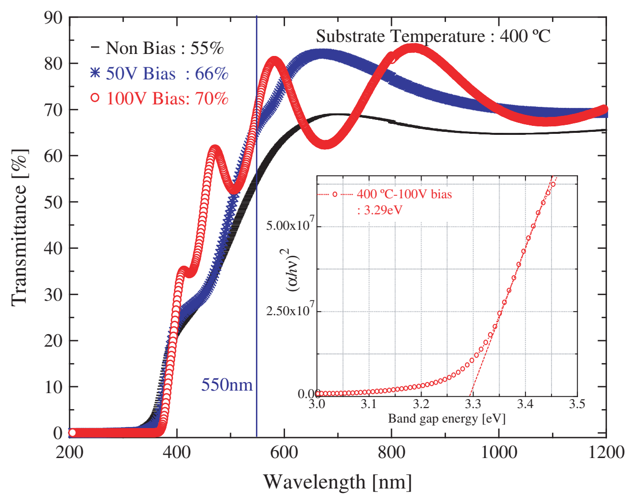

Fig. 4. Optical transmittance of $SrCu_2O_2$ thin films. (Substrate temp.:400 °C, films thickness −0 V:200 nm, −50 V:310 nm, −100 V: 351 nm.)

wide error bar range, one can see the increasing tendency according to the pulsed bias, especially in the electrical conductivity and mobility. The electrical conductivity and mobility of $SrCu_2O_2$ films increase from 0.04 S/cm and

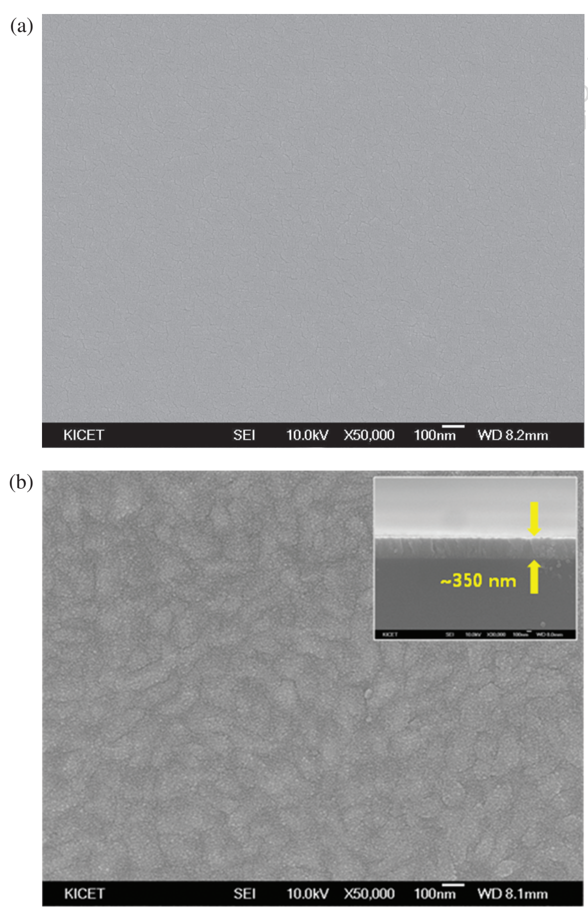

Fig. 5. SEM images of $SrCu_2O_2$ thin films. ((a) 400 °C/0 V $SrCu_2O_2$, (b) 400 °C/−100 V $SrCu_2O_2$.)

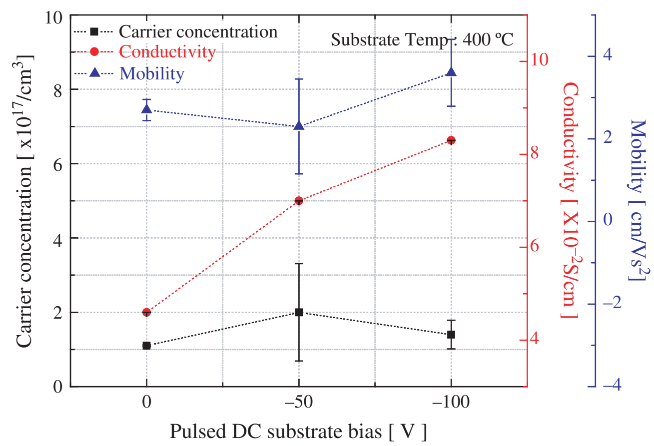

Fig. 6. Electrical properties of $SrCu_2O_2$ thin film at various substrate bias voltages. (Substrate temp: 400 °C.)

Table II. Electrical properties of $SrCu_2O_2$ thin films at various deposition conditions.

	Properties			
Sub temp.	Carrier concentration [/cm^3]	Mobility [cm^2/Vs]	Hall coefficient	Conductivity [S/cm]
300 °C				
100 V-bias	8.8×10^{16}	1.7	76	0.02
400 °C				
Non bias	1.1×10^{17}	2.7	59	0.05
50 V-bias	2×10^{17}	2.3	31	0.07
100 V-bias	1.4×10^{17}	3.6	44	0.08

2.7 $cm^2/V \cdot s$ to 0.08 S/cm and 3.6 $cm^2/V \cdot s$ with increasing the bias voltage. Within the author' knowledge, the value of 0.08 S/cm in the electrical conductivity is the highest one, when compared to those deposited by PLD and *e*-beam methods.[18, 19]

It is thought that, as bias voltage increases, the crystallinity (defects) is improved (decreased) and the grain size becomes large, and these result in the increased carrier number and the carrier mobility because of the decreased portion of the grain boundary in the electrically conducting paths. And this is the reason for the improved electrical conductivity. RF magnetron sputtering under unbalanced bipolar pulsed DC bias is thought to be a very useful method for crystallization and grain growth of the oxide thin films at relatively lower deposition temperature. Summary of the electrical properties of $SrCu_2O_2$ thin films were listed in Table II.

4. CONCLUSION

RF magnetron sputtering under unbalanced bipolar pulsed DC bias revealed a very useful method for crystallization and grain growth of $SrCu_2O_2$ thin films at relatively lower deposition temperature below 400 °C. The appearance of Cu phase above the applied pulse bias above −150 V is resulted from preferential re-sputtering of Cu atoms, compared to more heavy Sr atoms, and re-deposition occurs as the metallic Cu phase. The maxima at −100 V bias voltage in the deposition rates of $SrCu_2O_2$ films are thought to be resulted from the increased Cu re-sputtering rate according the bias voltage, and decrease in the deposition rate. XRD and SEM results confirmed that the crystallite size of the deposited $SrCu_2O_2$ films increased with increasing pulsed-DC bias voltage. The $SrCu_2O_2$ films deposited under the pulsed-bias of −100 V exhibited the highest conductivity of 0.08 S/cm and over 70% of transmittance at 550 nm. It is thought that, as the bias voltage increases, the crystallinity (defects) is improved (decreased) and the grain size becomes large, and these result in the increased carrier number and the carrier mobility because of the decreased portion of the grain boundary in the electrically conducting paths.

References and Notes

1. T. Nozawa, *Transparent Electronic Products Soon a Reality, Nikkei Electronics Asia* (**2007**).
2. E. Fortunato, P. Barquinha, A. Pimentel, A. Gonçalves, A. Marques, L. Pereira, and R. Martins, *Advanced Materials* 17, 590 (**2005**).
3. I. Hamberg and C. G. Granqvist, *J. Appl. Phys.* 60, R123 (**1986**).
4. C. G. Van de Walle, *Physical. Rev. Lett.* 85, 1012 (**2000**).
5. R. Wendt and K. Ellmer, *Surf. Coat. Technol.* 93, 21 (**1997**).
6. H. Kawazoe, M. Yasukawa, H. Hoyodo, M. Kurita, H. Yanagi, and H. Hosono, *Nature* (*London*) 389, 939 (**1997**).
7. H. Yanagi, H. Kawazoe, A. Kudo, M. Yasukawa, and H. Hosono, *J. Electro-Ceramics.* 4, 407 (**2000**).
8. A. Kudo, H. Yanagi, H. Hosono, and H. Kawasoe, *Appl. Phys. Lett.* 73, 220 (**1998**).
9. E. Bobeico, F. Varsano, C. Minarini, and F. Roca, *Thin Solid Films* 444, 70 (**2003**).
10. H. W. Seok, S. K. Kim, H. S. Lee, T. Y. Lim, J. H. Hwang, D. K. Choi, and K. H. Chai, *Mat. Res. Soc. Kor.* 20, 676 (**2010**).
11. P. J. Kelly and R. D. Arnell, *Vacuum* 56, 159 (**2000**).
12. D. I. Safi, G. W. Hall, and R. P. Howson, *Surf. Coat. Technol.* 99, 147 (**1998**).
13. C. H. Ma, J. H. Huang, and H. Chen, *Surf. Coat. Technol.* 133/134, 289 (**2000**).
14. P. J. Kelly, R. Hall, J. O'Brien, J. W. Bradey, P. Henderson, G. Roche, and R. D. Amell, *J. Vac. Sci. Technol.* A19, 2856 (**2001**).
15. J. Y. Wang, M. K. Ghantasala, and R. J. McLean, *Thin Solid Films* 517, 656 (**2008**).
16. K. G. Godinho, J. J. Carey, B. J. Morgan, D. O. Scanlon, and G. W. Watson, *J. Mater. Chem.* 20, 1086 (**2010**).
17. H. Ma, X. Hao, J. Ma, Y. Yang, S. Huang, F. Chen, Q. Wang, and D. Zhang, *Surf. Coat. Technol.* 161, 58 (**2002**).
18. A. Kudo, H. Yanagi, H. Hosono, and H. Kawasoe, *Appl. Phys. Lett.* 73, 220 (**1998**).
19. E. Bobeico, F. Varsano, C. Minarini, and F. Roca, *Thin Solid Films* 444, 70 (**2003**).

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