# Comprehensive Understandings on the High Dielectric Constant Insulating Layers for Alternating-Current Thin-Film Electroluminescent Devices

Yun-Hi Lee, Byeong-Kwon Ju, *Member, IEEE,* Dong-Ho Kim, and Myung-Hwan Oh, *Member, IEEE*

***Abstract*—We introduced thin-film electroluminescent cells (TFEL) with a new multilayered-$BaTiO_3$ layer for the low-voltage driven devices. We begin by simulating the basic parameters for TFEL devices in eletrostatic boundary condition and point out how the insulator parameters influences on the typical operating properties of the devices. Next, we performed the voltage accelerated breakdown testing of the multilayered-$BaTiO_3$ having both high dielectric constant and high breakdown strength. The time-zero-breakdown distribution is shown to be dependent on surface roughness, while the long-term failure studied by time-dependent-dielectric breakdown technique at high field is dependent on the bulk characteristics, i.e., transition layers within m-BT films. Thirdly, the TFEL devices were prepared using the multilayered-$BaTiO_3$ as dielectric materials. We observed a decrease of turn-on voltage with increasing thickness and the increase of the maximum over voltage. Finally, typical symmetric capacitance-voltage (*C–V*) and internal charge-phosphor field characteristics were obtained for the device with thin m-BT layers. With increasing thickness of m-BT the significant asymmetry with respect to the applied voltage polarity was observed. This is a main difference as compared with the symmetric characteristics of conventional TFEL devices with low dielectric constant insulators. The experimental results indicate the fact that a selection of the thickness of upper m-BT and their deposition process would strongly affect the interfacial characteristics as well as bulk characteristics of an as-grown ZnS : Pr, Ce layer.**

***Index Terms*—$BaTiO_3$, electroluminescence, insulating films, TFEL.**

## I. Introduction

THE INSULATORS in alternating current thin film electroluminescent (ACTFEL) cells should have high dielectric reliability as well as a high figure of merit in order to achieve both the low power consumption and the stable operation of the device. A large insulator capacitance increases the voltage drop across the phosphor layer, thus increasing the magnitude of the phosphor field [1]. A large phosphor field contributes effectively to the emission of deep interface traps into the phosphor conduction band and (a large phosphor field) enhances the acceleration process of the injected electrons as these electrons are transported across the phosphor. The large insulator capacitance also reduces the operating voltage.

The larger the breakdown field in insulating layers, the higher the applied voltage the device can withstand and the more reliable the device. Unfortunately, the high dielectric constant materials tend to have low breakdown field strength. Thus, we can imagine that one of the methods of increasing the dielectric constant while maintaining a large breakdown field is to use alternating layers of one material with a large breakdown field and another material with a high dielectric constant [2], [3]. When a polycrystalline-$BaTiO_3$ film (p-BT), having a high dielectric constant but relatively low breakdown field, was used as an insulating layer for electroluminescent cells, it was found that the efficiency of the device decreases because of the high leakage current of a p-BT layer. However, a recent work has shown that, by a new stacking method, multilayered-$BaTiO_3$ (m-BT) films can be fabricated where both the high dielectric constant ($>$100 at 1 KHz) and high dielectric breakdown strength ($>$dc 1 MV/cm) are achievable features [4]. Furthermore, the above study has presented that a m-BT film can be successfully applied to the lower insulating layer for highly efficient thin film electroluminescent (TFEL) cells.

The aim of this paper is to present the results of the electrical characterization that we have found in our experience to be particularly useful for the realization of the reliable high dielectric insulating films for the TFEL devices and additionally, comprehensive informations to enable the researchers in TFEL field to persist the on-going experimental efforts toward developing the low-voltage driven TFEL devices. The successful achievement for the devices relies heavily on the designing high dielectric materials, thin film processing technology for the materials and optimizing the structure for reliable TFEL devices. Prior to describing specific experimental trials, we begin by simulating the basic parameters for TFEL devices using eletrostatic boundary condition and point out how the insulator properties influence on the typical operating characteristics of the devices. Next, we attempt to evaluate the dielectric reliability of our new m-BT films using two techniques, time-zero-dielectric-breakdown (TZDB) and time-dependent-dielectric-breakdown (TDDB) [5]. We suggest here that the "transition layer" within m-BT be a figure of merit in determining whether a m-BT layer provides sufficient margins to guarantee dielectric reli-

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Y.-H. Lee, B.-K. Ju, and M.-H. Oh are with the Information Display and Nano-Devices Laboratory, Korea Institute of Science and Technology, Seoul, Korea (e-mail: lyh@kist.re.kr).

D.-H. Kim is with Yeungnam University, Kyungsan, Korea.

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ability. Results from capacitance-voltage ($C$–$V$) and internal charge ($Q_{\rm int}$)-phosphor field ($F_p$) analysis are used to investigate the effect of different thickness of m-BT's on the electrical behavior and the maximum overvoltage margins of our TFEL cells. The surface roughness estimated by atomic force microscopy was utilized to understand for the abruptness of the experimentally obtained $C$–$V$ curves before and after turn-on. Finally, we presented auger electron spectroscopy spectra of TFEL cells with different m-BT films, accounting for the effect of m-BT thickness on both interface between m-BT and ZnS : Pr, Ce. This result enables the explanation of strong asymmetric properties for the upper interface and helps to determine the usable structure for manufacturing reliable TFEL devices using high dielectric constant insulators.

## II. Fabrication and Characterization

In this work, all $BaTiO_3$ thin films were prepared by the rf-magnetron sputtering technique on glass (Corning 7059) coated with indium-tin-oxide (ITO) having a sheet resistance of about 20 ($\Omega/\square$). A 4-inch $BaTiO_3$ ceramic disk sputtering target with a 99.99% purity was used. The base pressure in the chamber was adjusted to $5 \times 10^{-5}$ Torr and the pressure during the deposition was maintained at 4 mTorr of an Ar and $O_2$(20%) gas mixture. The poly-BT thin films were deposited on the substrates heated at 550°C, after which the power to the substrate heater was turned off. Thus, nonpolycrystalline $BaTiO_3$ phases begin to grow on the naturally cooling p-BT layer. Here, it was confirmed that the substrate temperature was determined by

$$\frac{T(t)-T_{eq}}{550-T_{eq}} = 1 - \text{erf}[C(t-75)] \tag{1}$$

where, $T$ and $t$ denote, the substrate temperature and time after turning off the power heater, respectively. $T_{eq}$ is the equilibrium temperature of the unheated substrate during the deposition process, and for our system, the value was 10 0°C. The constant $C$ depends on the heat capacitance of the heating module and pressure in the processing chamber, and the value is 0.043. Although the cooling rate of substrate was not intentionally controlled, it would not be difficult to adjust the rate by using a cooling module. The thickness of single poly-BT thin film was about 200 nm and in the case of a group of multi-BT thin films, the thickness of underlying poly-BT layer was varied from 100 nm to 600 nm, while the thickness of the topmost amorphous $BaTiO_3$ (a-BT) layer was fixed to 100 nm. 100 nm-thick-aluminum top electrodes of 0.7 mm in diameter were formed onto the thin film by thermal evaporation and then the electric properties of the capacitors with metal-insulator-metal (MIM) structure [ITO/ multi-$BaTiO_3$(200, 400, 700 nm)/Al] were characterized.

The thickness of the prepared thin film was measured by stylus of TENCOR $\alpha$-200 model. The crystallinity of the thin films was studied by X-ray diffraction (XRD) measurements. Ramp-voltage-stressed current–voltage ($I$–$V$) (TZDB) and constant-voltage-stressed $I$–$t$ (TDDB) characteristics were obtained by a fully automated Keithley 237 high voltage source and measuring unit. In this measurement the breakdown field of capacitor was defined as the applied field at which the leakage current exceeded 1 mA. Time-to-breakdown was monitored over the time interval of 0 $\sim$ 1000 seconds. In order to measure dielectric reliability of our multilayerd-$BaTiO_3$, a ramp-voltage-stresses $I$–$V$ (TZDB) and constant-voltage-stresses $I$–$t$ (TDDB) characteristics were taken by a fully automated Keithley 237 high voltage source and measure unit. In this measurement the breakdown field of M (ITO)-I (m-BT)-M (Al) capacitor was defined as the applied field at which the leakage current exceeded 1 mA. Time-to-breakdown was monitored over the time interval of 0–1000 s for the 180 dot capacitors with a dot area of $3.8\times10^{-3}$ cm$^2$. An impedance analyzer (HP 4192A) was used to obtain ac dielectric properties such as dielectric constant and dielectric loss as a function of the applied frequency for the m-BT.

TFEL devices were fabricated in the stack configuration in which an electron-beam evaporated ZnS : Pr, Ce layer was sandwiched between the m-BT layers which were contacted by a bottom indium thin oxide (ITO) and a top aluminum (Al) electrode. The ZnS : Pr, Ce phosphor thickness was approximately constant for all the EL devices. The m-BT layers used as upper and lower insulators were about 200, 400, and 700 nm in thickness. The symmetric ac TFEL cells of ITO/m-BT (200, 400, 700 nm)/ZnS : Pr, Ce (450 nm)/m-BT (200, 400, 700 nm)/Al are referred to as "s1," "s2," and "s3," respectively, in the remainder of this paper.

$C$–$V$ and $Q$–$F_p$ analyzes were accomplished using both a programmable arbitrary waveform generator (HP model 33 120A) and a high-voltage amplifier (Apex model PA 85). All of the electrical data were obtained using a digitizing oscilloscope (Tektronix model 510A). The $C$–$V$ and internal charge ($Q_p$)-phosphor field ($F_p$) characteristics were obtained by plotting the dynamic capacitance as a function of the voltage across the EL devices and their analyses were made by the $Q_p(t)$ and $F_p(t)$ equations [6], [7].

$$Q_{\rm int}(t) = \frac{(C_i + C_p)}{C_i} C_s v_3(t) - C_p[v_2(t) - v_3(t)] \tag{2}$$

$$F_p(t) = \frac{1}{d_p}\left(\frac{C_s v_3(t)}{C_i} - [v_2(t) - v_3(t)]\right) \tag{3}$$

where $C_i$ and $C_p$ are the insulator and phosphor capacitances, respectively. Note that in order to obtain to a good estimate of $Q_{\rm int}(t)$, $C_i$, and $C_p$ must be accurately known. $Q(t)$ curves are primarily used as the input data for $Q$–$F_p$ and $Q_{\max}$–$V_{\max}$ assesement. The difference between a $Q_{\rm int}(t)$ curve and a $Q_{\rm ext}(t)$ curve involves rescaling and subtraction of displacement charge. $Q_{\rm ext}(t)$ is the transient charge measured externally with respect to the phosphor of an ACTFEL device. From a device physics perspective, it would be very useful to know the behavior of the internal charges between insulator/phosphor interfaces, $Q_{\rm int}(t)$.

## III. Results and Discussion

### A. Simple Survey on the Effect of the Insulator Properties on the TFEL Devices

When insulating layer is present and the applied field is pulsed through the threshold field, only a limited number of charge per unit area can pass through the phosphor layer,

depending upon the capacitance of the insulating layer [8]. In this way the dissipation or heating is limited to an acceptable level throughout the phosphor film and catastrophic failure is essentially eliminated.

Therefore, we begin by examining on the insulator limitation required in order for an AC TFEL device to have charge injection [8]–[10]. When a voltage is applied across the device such that the voltage $V_a$, then the phosphor conducts until the electric field in the phosphor is reduced to $E_{pth}$ by the charging of the capacitor, i.e., insulating layers. Initially, the applied voltage $V_a$ is distributed according to the simple electrostatic continuity condition

$$\varepsilon_i E_{ith} = \varepsilon_p E_{pth} \tag{4}$$

where $E_{ith}$ is the insulator threshold field when the phosphor electric field reaches its threshold value. Here, the interface charge density is negligible, or at least small, at threshold. Notice the fact that if the insulator breakdown field $E_{ibd}$ is less than the value of $E_{ith}$, the insulator cannot be used in conjunction with that the particular phosphor layer, regardless of the insulator or the phosphor layer thickness.

Fig. 1 shows a log-log plot of $E_{ith}$ versus $\varepsilon_i$ obtained from (4). For each phosphor layer characterized by dielectric constant $\varepsilon_p$ and $E_{pth}$, the result is a straight line with slope of unity. Insulating layers with properties which lies to the left of the line for a given phosphor are not usable for that the particular phosphor material; only regions of $E_{ith} - \varepsilon_i$ plane to the right of the line define where an insulator material is usable. This simple calculation is particularly interesting since insulating layers with very small $E_{ith}$'s may be employed as TFEL insulators if the insulator possesses a large dielectric constant. However, it is important to note that the lines shown in Fig. 1 define only the minimum required insulator properties and $E_{ibd}$ should be larger than the minimum value suggested by the $E_{ith} - \varepsilon_i$ curve. Additionally, the value of $E_{ibd}$ required for TFEL device applications depends on the operating voltage requirement, i.e., the threshold applied voltage, $V_{ath}$, and the overvoltage, $V_{over}$, which is the applied voltage in excess of the threshold voltage.

We do not wish to pursue any further, but merely state that there is a consideration for the insulating layer which can determine to the minimum operation of TFEL device and that is defined within $E_{ibd}$ of insulating layer is larger than the value of $E_{ith}$.

Next, in order to obtain relationship between the threshold applied voltages and the phosphor and insulator variables, an initial condition in which there is no polarization charge at the interface is assumed. Also, an ideal field-clamping case is assumed in which the phosphor electric field remains constant at $E_{pth}$. At the threshold for the injection, the applied voltage, $V_{ath}$, is capacitively distributed according to

$$V_{ath} = V_{ith} + V_{pth} \tag{5}$$

where $V_{pth}$ and $V_{ith}$ are the phosphor and the insulator field at threshold, respectively. Reassuming a uniform field across the phosphor, $V_{pth}$ can be calculated as

$$V_{pth} = d_p E_{pth}. \tag{6}$$

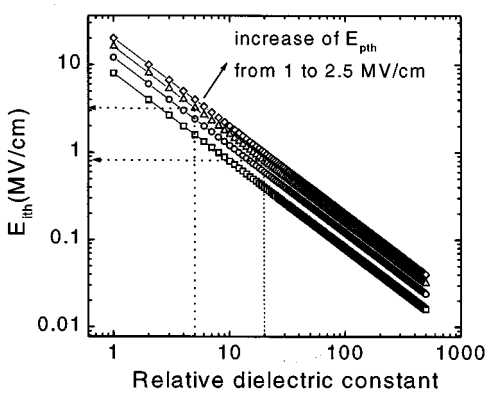


Fig. 1. Plot of the insulator field at the onset of phosphor conduction, $E_{ith}$, for $d_i = 250$ nm and $d_p = 500$ nm.

Since we assume that there is no polarization charge, $V_{ith}$ can be calculated as follows, assuming an uniform field within the insulator and assuming that (3) holds,

$$V_{ith} = \frac{\varepsilon_p d_i}{\varepsilon_i} E_{pth}. \tag{7}$$

Thus, $V_{ath}$ is to be

$$V_{ath} = \left( \frac{d_i \varepsilon_p}{\varepsilon_i} + d_p \right) E_{pth}. \tag{8}$$

A major interest in TFEL device, which we have ignored up to this point, is the brightness level and the magnitude is determined by the amount of overvoltage, $V_{over}$, that is applied in excess to the threshold voltage, $V_{ath}$. Considering operating mechanism for the TFEL device, the overvoltage is dropped only across the insulator, since it is assumed that above threshold the phosphor voltage is clamped at the threshold, $V_{pth}$. Therefore, the relationship between the maximum overvoltage, $V_{\max over}$ and the phosphor and insulator variable is

$$V_{\max over} = d_i (E_{ibd} - E_{ith}) = d_i \left( E_{ibd} - \frac{\varepsilon_p}{\varepsilon_i} E_{pth} \right). \tag{9}$$

This insulator-limited overvoltage arises due to the finite breakdown field of the insulator. At voltages above this maximum overvoltage, the insulator breaks down and the TFEL device catastrophically burns out. The overvoltage is known to be about 40V for commercial displays. In order to minimize frequent burn out problems, the TFEL device should be designed with $V_{\max over}$ larger than 40 V.

To see the effect of the $E_{ibd}$ on the overvoltage margin $V_{\max over}$, (9) is rearranged into the following form:

$$E_{ibd} = \frac{V_{\max over}}{d_i} + \frac{\varepsilon_p}{\varepsilon_i} E_{pth}. \tag{10}$$

From (10), $E_{ibd}$ can be found for a particular phosphor material by setting $V_{\max over}$ to a desired value. Fig. 2 shows a plot of $E_{ith}$, $E_{ibd\,40}$, and $V_{ath}$ as the function of $\varepsilon_i$, where $E_{ibd\,40}$ refers to the required $E_{ibd}$ necessary to obtain a $V_{\max over}$ of 40 V. Here, $E_{ith}$ refers the insulator field at the onset of conduction and this is the minimum $E_{ibd}$, and $E_{ibd\,40}$ refers to the required $E_{ibd}$ necessary to obtain a $V_{\max over}$ of 40 V. The distinct features of this are as follow: for a set of phosphor properties,

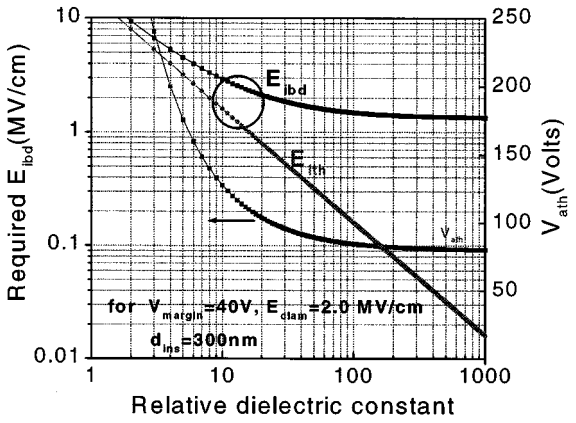


Fig. 2. Effect of the $V_{\max over}$ on the required insulator breakdown voltage. The $V_{\max over} = 40$ V, $d_i = 250$ nm, $\varepsilon_p = 20$, $d_p = 500$ nm, and $E_{pth} = 5$ MV/cm.

$E_{ith}$ is always smaller than $E_{ibd\,40}$ and unlike the plot of $E_{ith}$ which continuously decreases as $\varepsilon_i$ increases, $E_{ibd\,40}$ saturates for $\varepsilon_i \leq 1000$. In fact, for $\varepsilon_i \leq 1000$, $E_{ibd\,40}$ exceeds $E_{ith}$ by an order of magnitude. This arises because as $\varepsilon_i$ becomes large, the second term of (9) become very small, and $E_{ibd}$ saturates to $V_{\max over}/d_i$ (1.6 MV/cm).

The preceding analysis indicates that for a large value of $\varepsilon_i$, $V_{ath}$ depends only on the $d_pE_{pth}$ product and $V_{\max over}$ depends only on the $d_i$, $E_{ibd}$ product. As $\varepsilon_i$ decreases, $V_{ath}$ increases and $V_{\max over}$ decreases. Therefore, the lower limit of $V_{ath}$ and the upper limit of $V_{\max over}$ are described by

$$V_{ath} \geq d_pE_{pth} \quad \text{and} \quad V_{\max over} \leq d_iE_{ibd}. \tag{11}$$

Thus, we have concluded that for both device operation stability and turn-on voltage, in order to have a sufficient satisfaction, the value of the insulator breakdown field must be maximized for the same thickness of insulating layer. Here, it is important that the multilayered high dielectric insulating layer developed in this work for the TFEL device falls on the region bounded by the $E_{ith}$ and $E_{ibd\,40}$ lines sufficiently.

### *B. Characteristics of m-BT Films Under the Accelerated DC Stress*

Fig. 3 shows a close look at breakdown with scanning electron microscope (SEM) measurements for three different types of m-BT. SEM pictures of the breakdown site clearly show the m-BT destroyed by thermal run-away effects. The m-BT with a thicker p-BT underlayer has deeper hole and severe cracking.

As generally known, the breakdown is studied under the accelerating test condition of high field stress resulting in practically measurable breakdown time [11]. In order to extrapolate the dc acceleration results to field conditions as are found in common ac EL device application, a knowledge of TDDB behavior is necessary. A probability distribution function that fits breakdown data can be used to predict failure rates as a function of time. Gaussian (or Normal) distribution is bell-shaped curve and used for process monitoring and control charts. Weibull distribution is similar to log Normal distribution and appropriate for accelerated life testing as well as this distribution predicts early failure.

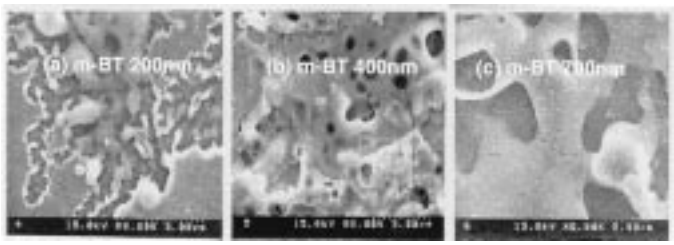


Fig. 3. SEM photographs for the breakdown site for the m-BT with different thickness.

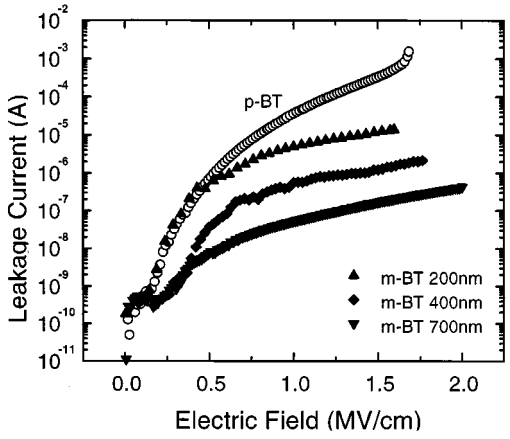


Fig. 4. DC leakage current—Applied field curves for the m-BT with different thickness after about 10 minutes aging.

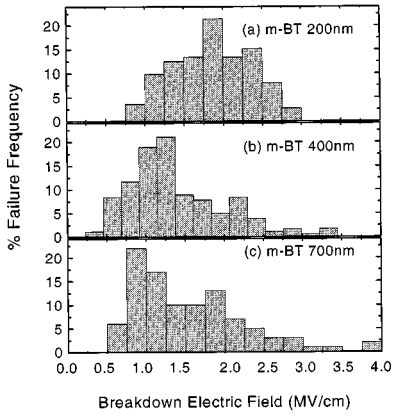


Fig. 5. Breakdown field histogram for the m-BT with different thickness.

Figs. 4 and 5 show time-zero current ($I$)-Electric field ($E$) characteristics and the time-zero-breakdown distribution for three types of m-BT at constant time, respectively. The leakage current at the fixed stress field decreased as thickness of m-BT increased and the most frequent breakdown of 700 nm-thick m-BT occurred at the lower electric field when compared with those of the thinner m-BTs. Furthermore, Fig. 3 of TZDB results with ramp-voltage-stressed for the 400 nm- and 700 nm-thick m-BT films shows typical Weibull distribution applicable to failure in good insulating films [12]. Fig. 6 shows typical cumulative Weibull plot for three types of m-BT. Here, the horizontal axis represents the stress time $t$ and the vertical axis represents the cumulative failure percent. Note that the lifetime increases slightly as the thickness of m-BT gets thicker.

It is generally accepted that an extrinsic breakdown is the largest reliability problem for the oxide insulating film and that the extrinsic breakdown is related to defects existing, which are in the film before the electric stress, i.e., process-induced defects such as particle, surface asperities and structural weakness [11], [13]. Here, in order to study the factor influencing the results presented in Figs. 3–6, we investigate especially the interface roughness effect on the peak occurrence of time zero breakdown and the layered structural effect of m-BT, i.e., thickness of a transition layer between polycrystalline-BT (p-BT) and amorphous-BT (a-BT), on the leakage current and TDDB properties with increasing thickness. Fig. 7 shows AFM images for the surface of m-BT films. Root-mean-square (rms) roughness estimated from these results increases with increasing thickness of m-BT, indicating that the roughness of M-BT is increased by forming a thicker p-BT underlayer. Thus, based on the explanation that the nonuniformity and the sharp points are assumed to be main sources of the weak spot under the dc electric field of 1–2 MV/cm, the trends of Figs. 5 and 6(a) can be easily understood.

### *C. Role of the Transition Layer within m-BT on the Long-Life-Breakdown Behavior of m-BT Capacitors*

On the other hand, the reduced leakage current with increasing thickness as shown in Fig. 4 was not explainable considering the increase of rms roughness. Here, it should be emphasized that the increase of p-BT thickness is always accompanied with the increase of the transition layer between p-BT and a-BT layers as shown in [5]. The decrease of leakage current at dc high stress voltage is most likely due to the thicker transition layer with increasing the p-BT thickness, supporting the previous suggestion that the transition layer act as resistive against electron movement.[4]

In same context the shift of Weibull plot toward to longer time with increasing thickness in Fig. 6(b) can be attributed to both the stress relaxation and a reduction of moving oxygen vacancies by the widening of the transition region between p-BT and a-BT.

### *D. Capacitance-Applied Voltage ($C$–$V$) and Internal Transferred Charge-Internal Phosphor Field ($Q_{\rm int}$-$F_p$) Characteristics of TFEL Cells Under Bipolar Pulse Drive*

Note that the $C$–$V$ curve of our EL devices shifts in a slightly nonrigid manner with respect to M-BT thickness as shown in Fig. 8(a). This nonrigid shift in the $C$–$V$ curve indicates that the interface state density in the preclamping field regime [6], $Q_{ss}$, is dependent on the m-BT thickness. The variation of rms roughness with increasing thickness of m-BT is seen as the source of the change of $Q_{ss}$. Note from the figure that $C_i$ (Al plus) is greater than $C_i$ (Al minus). A family of $C$–$V$ curves for the devices with 400 nm-thick m-BT and 700 nm-thick m-BT are displayed as a function of operating voltage in Fig. 8(b) and (c), respectively. Perhaps the most unusual aspects of the curves shown in these figures are the significant asymmetry with respect to the applied voltage polarity for all symmetric devices fabricated in this work. Furthermore, the most significant asymmetry was observed at a "s3" device. Tentatively, we attribute the observed polarity-dependent $C_i$ to the existence of different

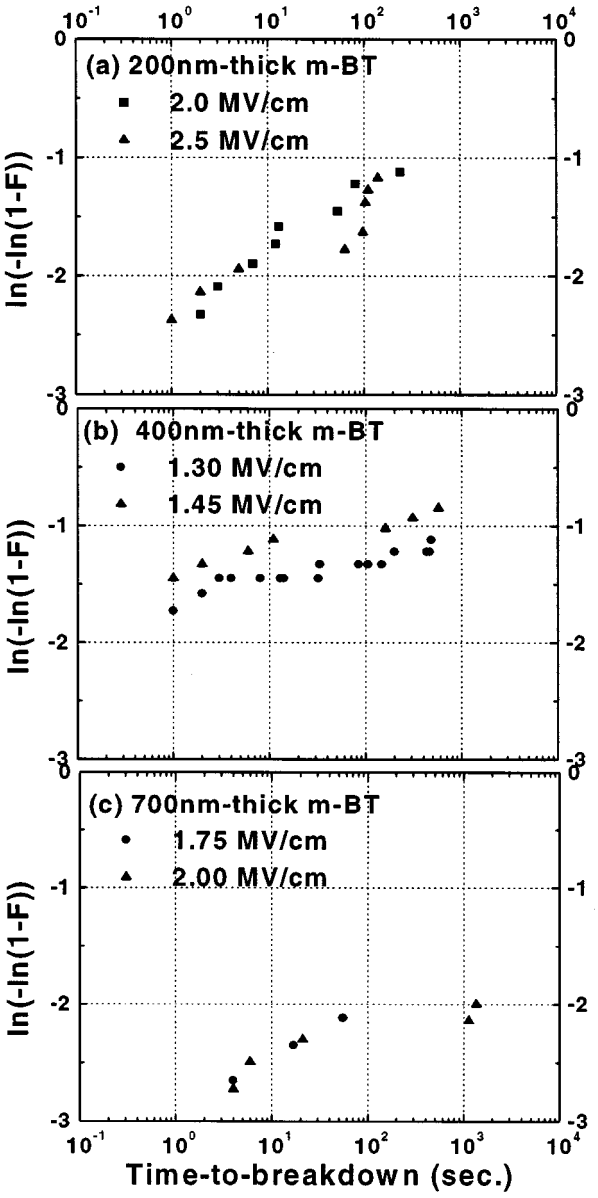


Fig. 6. TDDB time-to-failure distribution for m-BT with different thickness under negative bias. Usually the cumulative distribution function ($F(t)$) is plotted and the breakdown data are often approximately Weibull distributed. $F(t) = 1 - \exp(-t/\eta)\beta$ where $t$, $\beta$, and $\eta$ represents time, shape parameter, and characteristic time to failure.

interface state distribution at the two interfaces between the phosphor and insulators and thus, interface roughness.

Next, we present the typical results of $Q_{\rm int}$–$F_p$ measurements for the s1, s2, and s3 devices in Fig. 9. There are several differences between these devices. At first, much more conduction charge is transported across the phosphor in the s3 device. This is a consequence of the larger dielectric capacitance of m-BT of the s3 device (i.e., $\sim$95) compared to those of s1($\sim$20) and s2(55 $\sim$ 65). Secondly, contribution of relaxation charge to conduction charge is larger in "s2" and "s3." Much of the charge across the phosphor of s2 and s3 appears to reside in deep traps such that it is emitted from these traps when the external bias is maintained at peak voltage. Thirdly, the s1, s2 and s3 devices exhibit a distinct steady state field of $F_{ss}^{+}$ (Al plus). In contrast, $F_{ss}^{-}$ of s2 and

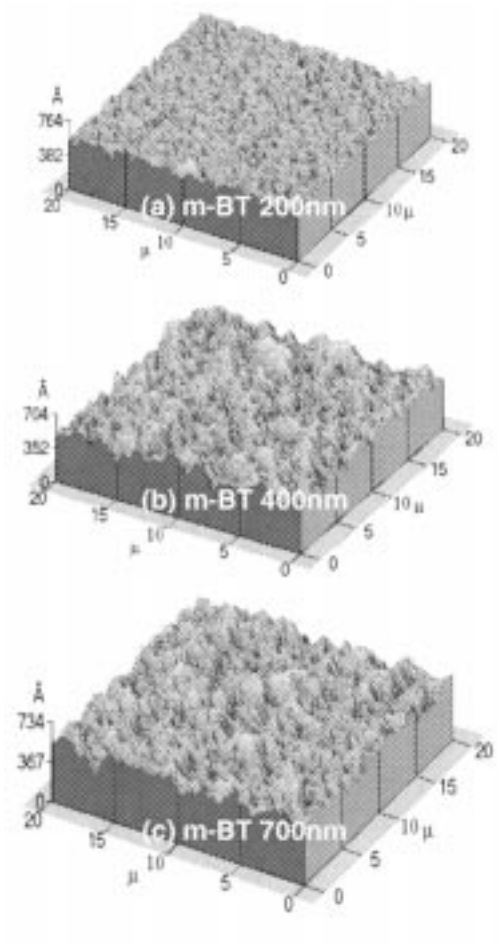


Fig. 7. AFM images for the topmost surface of m-BT with different thickness.

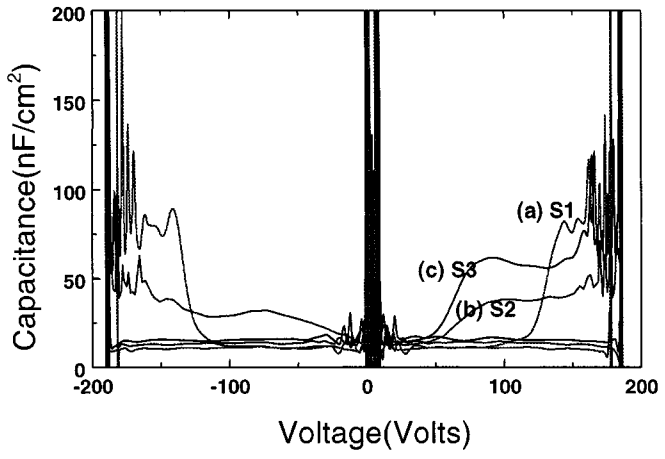


Fig. 8. Capacitance-voltage curves of EL devices with different thickness of m-BT.

s3 at Al minus is not well-defined as well as the magnitude and shape as shown in Fig. 8. Finally, the $Q_{\rm int}$–$F_p$ plot at Al minus is nearly symmetric for the s1 device but strongly asymmetric for "s2" and "s3."

From the observed results, we suppose that while the bottom interface is relatively independent of the lower m-BT layer, the top interface is severely affected by the thickness of m-BT or

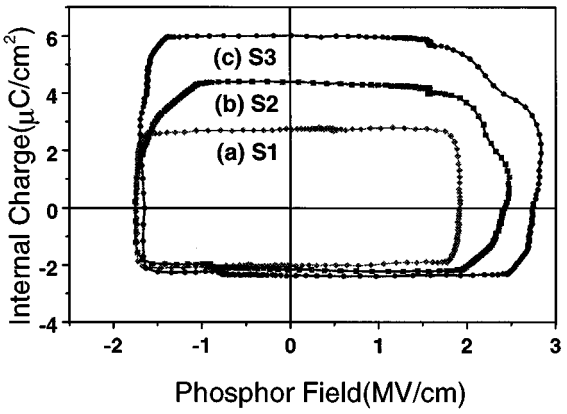


Fig. 9. Internal charge ($Q_{\rm int}$)-phosphor field ($F_p$) loops of the s1, s2, and s3 devices.

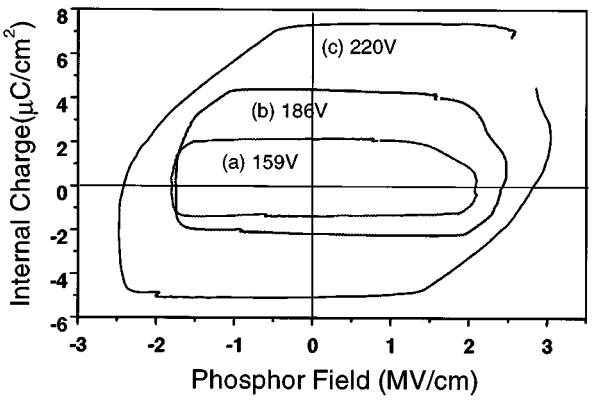


Fig. 10. Internal charge ($Q_{\rm int}$)-phosphor field ($F_p$) loops as a function of maximum applied voltage.

their processing. Other evidence is shown in Fig. 10. $F_{ss}^{+}$ (ITO minus) for the "s2" is nearly constant except at larger $V_{\max}$ ($V_{\max} = 220$ V) while $F_{ss}^{-}$ (i.e., electrons emitted from the Al side interface) increases continuously with increasing $V_{\max}$. The trends exhibited by $F_{ss}^{+}$ are attributed to an interface state distribution of the bottom interface which sharply increases at a certain energy to a large density as compared to those of the top interface. This contention, that the interface state distribution is abrupt for the bottom interface, is supported by the $Q_{ss}$ trends shown in Figs. 5 and 6 and shaper interfacial profiles confirmed by AES analysis.

In contrast, the $F_{ss}^{-}$ trends shown in Figs. 10 and 11 indicate that field-clamping does not occur when electrons are emitted from the top interface. It is possible that this absence of field-clamping arises from shallow interface states that are distributed over a large range of energy.

Finally, to confirm the internal asymmetric properties of the devices with the symmetric material and thickness, we measured in-depth profile using AES method. Fig. 11(a)–(c) shows a whole concentration profile of the composing ions for the "s1," "s2" and "s3" devices, respectively. The result showed three features; first, the amount of Zn and Ba was slightly higher than S and O at the lower interface between lower m-BT and ZnS : Pr, Ce, regardless of the thickness of m-BTs. Second, differing from the lower interface, the ratio of Zn to S at the upper interface

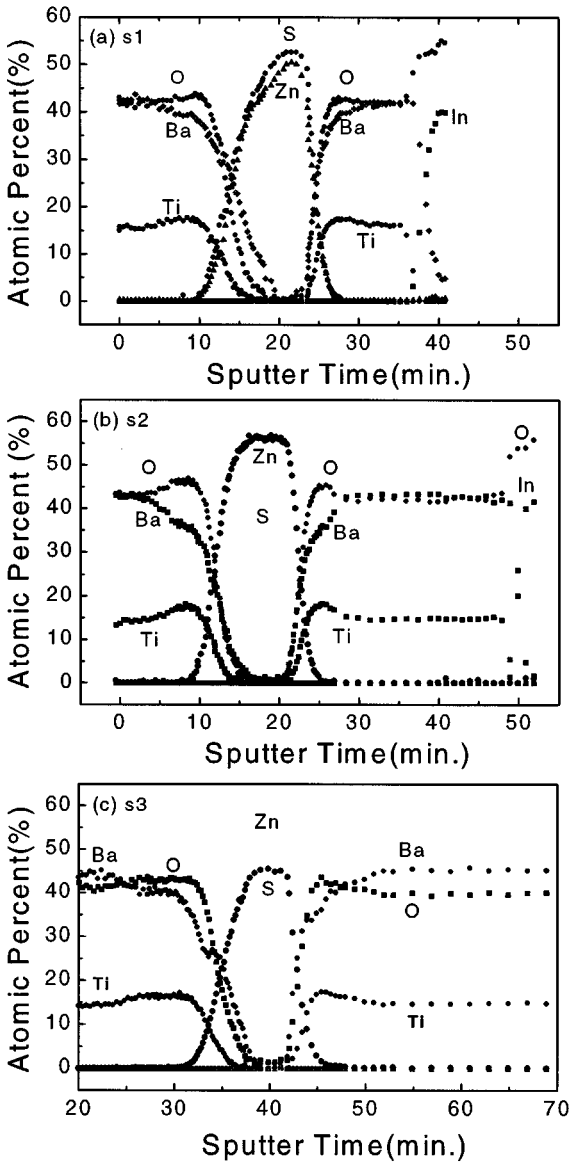


Fig. 11. AES depth-profile for the EL structure with different thickness of m-BT.

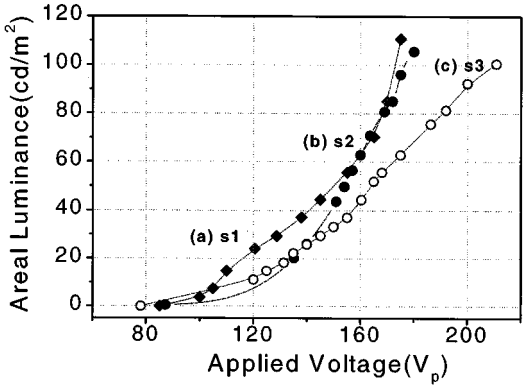


Fig. 12. Luminance-applied voltage curves of the s1, s2, and s3 devices, respectively. Prior to starting measurement, EL devices were aged for about 90 min to stabilize. The waveform applied is nearly symmetric bipolar pulses of rectangular shape with a pulse with of 50 $\mu$sec and a frequency of 1 kHz.

was significantly varied from sulfur rich "s1" to sulfur deficient "s2" and "s3." As frequently observed, the off-stoichiometric ZnS, i.e., Zn excess (or sulfur deficient) was easily resulted from phosphor process though controllability was dependent on the PVD or CVD. Here, it is important that the ratio of S/Zn of "s1" device was higher than 1 after the deposition of the upper insulator followed by vacuum-anneal of ZnS while that of "s2" and "s3" was lower than unity. Also, note that at the top interface region the layered interface was formed such as Ba-rich m-BT, Zn-rich region and their mixed region. It was common to the s2 and s3 devices.

### *E. Luminance-Applied Voltage Characteristics of TFEL Cells Using the m-BT Insulator*

The luminance-applied voltage curves of the "s1," "s2" and "s3" devices are shown in Fig. 12. This figure shows two distinct features. First, a decrease of turn-on voltage with increasing m-BT thickness, i.e., dielectric capacitance. Essentially, the reason for this result is that with increasing insulator dielectric capacitance there is an increasing portion of the applied voltage which appears across the phosphor layer, when the same value of $V_a$ was applied at the devices. Second, the increase of maximum over voltage margin with increasing m-BT thickness. It is proposed that thicker insulating layer has a beneficial influence on the operation reliability of TFEL devices.

An asymmetric TFEL device with different thick lower and upper m-BT is further necessary for a complete evaluation of TFEL devices using these dielectrics.

## IV. Conclusions

In this work, we applied successfully a high dielectric constant material for the insulator of low voltage-driven white light emitting ac TFEL devices. The time-zero and time-dependent dielectric breakdown technique was employed as a method of investigating dielectric reliability for TFEL. The value of the most frequent breakdown field was lowered with increasing thickness of m-BT, while distribution of the breakdown field was narrowed for thinner films. Analysis of the surface roughness for the m-BT confirmed that the time-zero breakdown mechanism is related to the rms deviation of roughness. The reduced dc leakage current at the thick m-BT and the long-time to failure were related to the presence of a wide transition layer formed between poly- and amorphous-BT. Therefore, we suggest that the width of "transition layer" in m-BT be a figure of merit in determining whether a m-BT layer provides sufficient margins to guarantee dielectric reliability.

For our symmetric TFEL devices using the high dielectric layers, the most distinct feature of the $C$–$V$ and $Q$–$F_p$ characteristics is the significant asymmetry with respect to the applied voltage polarity. Specially, the top interface is severely affected by the type of m-BT whereas the bottom interface is relatively independent of the lower dielectric layer. The luminance-voltage characteristics show two distinct features; a decrease of turn-on voltage with increasing m-BT thickness, i.e., dielectric capacitance and the increase of maximum over voltage margin

with increasing m-BT thickness. It is proposed that thicker insulating layers have a beneficial influence on the operation reliability of TFEL devices.

The fabrication of asymmetric TFEL devices with different thick lower and upper m-BT and TDDB measurement of phosphor film is further necessary for a complete evaluation of TFEL devices using these dielectrics.

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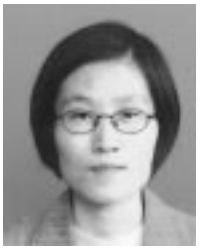

**Yun-Hi Lee** was born in Injae, Korea, on February 5, 1963. She received the M.S. and Ph.D. degrees in physics from Korea University at 1987 and 1994, respectively.

In 1988, she joined the Korea Advanced Institute of Science and Technology (KAIST), Seoul, where she was engaged in the development of flat panel display as Research Scientist. Since 1994, she has been a Senior Research Scientist of KAIST. Her research interests include thin film EL device physics, carbon nanotube devices and field emission displays.

Dr. Lee is a member of Society for Information Display (SID, USA), Korean Physical Society, and Korea Institute of Electrical Engineering (KIEE).

**Byeong-Kwon Ju** (M'99) was born in Jechon, Republic of Korea, on July 3, 1962. He received the M.S. degree in electronics engineering from University of Seoul in 1988 and Ph.D. degree in semiconductor engineering from Korea University in 1995.

In 1988, he joined the Korea Advanced Institute of Science and Technology (KAIST), Seoul, where he was engaged in development of mainly silicon micromachining and microsensors as a Research Scientist. In 1996, he spent six months as a Visiting Research Fellow at Microelectronics Center, University of South Australia, Australia. Since 1995, he has been a Senior Research Scientist of KAIST with his main interest in field emission display (FED) and silicon micromachining (MEMS).

Dr. Ju is a Member of the Society for Information Display (SID), Korea Institute of Electrical Engineering (KIEE) and Korean Sensors Society.

**Dong-Ho Kim** was born in Taegu, Korea, on January 6, 1957. He received the B.S. degree in physics from Seoul National University, Seoul, Korea, in 1979; the M.S. degree in physics from the Korea Advanced Institute of Science and Technology (KAIST), in 1981; and the Ph.D. degree in condensed matter physics from the University of Minnesota, Minneapolis, in 1989.

From 1989 to 1992, he was with Argonne National Laboratory, and from 1992 to 1994, he was with the Korea Institute of Science and technology (KIST) as a Senior Research Scientist. Currently, he is an Associate Professor, Department of Physics, Yeungnam University, Kyungsan, Korea. His research interests include vortex dynamics in high temperature superconductor, electrolumines

cent devices, and device physics of carbon-nanotube. Dr. Kim is a member of the American Physical Society, the Korean Physical Society and Korean Sensors Society.

**Myung-Hwan Oh** (M'99) was born on June 10, 1943. He received the B.S. and M.S. degree in electrical engineering from Seoul National University, Korea, in 1965 and 1972, respectively, and the Ph.D. degree in electrical engineering from Paul Sabatier University, Toulouse, France, in 1979.

Since 1967, he has been with the Korea Institute of Science and Technology (KIST) and is now Principal Research Scientist. His research interests include electroluminescent devices (TFELD), field emission display (FED), metal-oxide semiconductors, and sillicon micromachining.

Dr. Oh is a Member of the Society for Information Display (SID), and Korea Institute of Electrical Engineering (KIEE).