Available online at www.sciencedirect.com
SCIENCE DIRECT®
Physica B 334 (2003) 9–12
PHYSICA B
www.elsevier.com/locate/physb

Simple approach to fabricate microgated nanotubes emitter with a sidewall protector

Yoon-Taek Jang[a,b,*], Chang-Hoon Choi[a], Byeong-Kwon Ju[a], Jin-Ho Ahn[b], Yun-Hi Lee[c]

[a] *Microsystem Research Center, Korea Institute of Science and Technology, Seoul 136-791, South Korea*
[b] *Department of Materials Science & Engineering, Hanyang University, Seoul 133-791, South Korea*
[c] *Department of Physics, Korea University, 39-1, Hawolkog-dong, Seoul 136-701, South Korea*

Received 18 September 2002; received in revised form 18 September 2002; accepted 16 December 2002

Abstract

We successfully fabricated microgated nanotubes emitter using nanotubes directly grown on the substrate by the thermal CVD method. In order to reduce the leakage current due to flowing current along nanotubes grown on the sidewalls of the gate hole, we suggested the very simple processing step for fabricating sidewall protector using a parting layer that is generally used in metal tip process. The field emission properties imply a turn-on gate voltage of 52 V and an emission current of 1.7 μA at 100 V. The sidewall protector has an effect on reducing gate current by suppressing the growth of nanotubes on sidewall. The emission current fluctuation was ±10% over 2600 s.

PACS: 85.45.Db

Keywords: Carbon nanotube; Selective growth; Field emission; Triode emitter

Carbon nanotubes feature interesting electrical, chemical, and mechanical properties. Especially, due to their extreme aspect ratios, nanotube emitters feature large local field enhancement and thus yield considerable field emission currents at relatively low applied voltages. Nanotubes have a strong potential to be applied to field emitters including flat panel displays, cathode-ray tubes backlight for liquid crystal displays, and outdoor displays [1–4].

Among several types of field emitter using carbon nanotubes, the microgated field emitter using carbon nanotubes directly grown into micron holes is advantageous for small area electron source such as microwave generator and microdisplay to reduce scale of a unit device. Although several groups demonstrated the laboratory-type field emission array (FEA) using directly grown nanotubes, there are a few technical problems to be solved, such as process optimization to lower the gate voltage, i.e., the problem of damaging the gate electrode and the controlled growth of nanotubes [5–8]. Our group has reported experimentally the microgated nanotubes FEAs using an easy, economic process

*Corresponding author.
E-mail addresses: ytjang@kist.re.kr (Y.-T. Jang), yh_lee@korea.ac.kr (Y.-H. Lee).

0921-4526/03/$ - see front matter
doi:10.1016/S0921-4526(02)02668-6

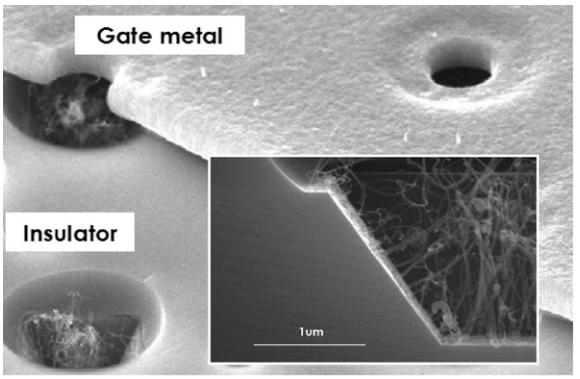
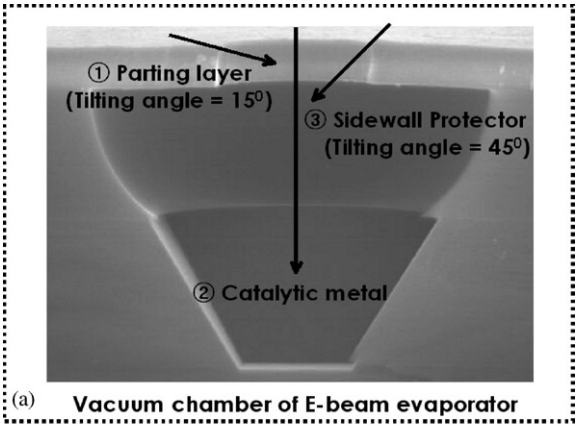


Fig. 1. The top view of the laboratory-type FEA using directly grown nanotubes. The inset shows the nanotubes grown on sidewall of gate holes.

commercialized for vacuum microelectronic devices. In addition, fine nanotubes wires with a finite three-dimensional structure were successfully grown on selected micrometer-scale areas [9,10].

Fig. 1 shows the top view of the laboratory-type nanotubes FEA. One pixel consist of 900 holes in area of $300\,\mu m \times 300\,\mu m$. The spacing between centers of hole is about $10\,\mu m$. Nanotubes were multi-wall nanotubes with an outer diameter range from 15 to 20 nm and well located at the center of holes. The inset of Fig. 1 shows the cross-sectional image of the sidewall of FEA. Nanotubes were randomly grown on sidewall because we tried to selectively deposit the catalytic metal at center of holes but occasionally observed catalytic metal deposited on the sidewall of gate holes. The biggest factor in increasing a gate current of microgated FEA using nanotubes was to flowing current along nanotubes grown on the sidewalls of the gate hole. We could not simultaneously control the length of nanotubes at both of center and sidewall of holes. Though nanotubes at the center of holes were not contacted with gate electrode, nanotubes on the sidewall could be contacted with gate. In order to reduce the leakage current due to flowing current along nanotubes grown on the sidewalls of the gate hole, we adopted new process scheme such as sidewall protection. David S.Y. Hsu reduced leakage current using nanotubes inside open trench with oxide [11]. In their work, low-pressure chemical vapor deposition (LP-CVD) and reactive ion etching (RIE) was used to fabricate oxide spacer lining sidewall of gated aperture and to remove catalyst of part that nanotubes should not be grown. This is complicated process that some step should be added in existent process. In our work, we easily fabricated oxide spacer and catalytic metal inside the emitter holes using a parting layer that is generally used in metal tip process.

The details of our process are the same as spindt process until formation of parting layer [12,13]. We continuously deposited parting layer, catalytic metal, and sidewall protector by changing the deposition angle without breaking vacuum of process chamber as shown in Fig. 2(a). After parting layer deposition, catalytic metal was deposited instead of metal tip. Then sidewall



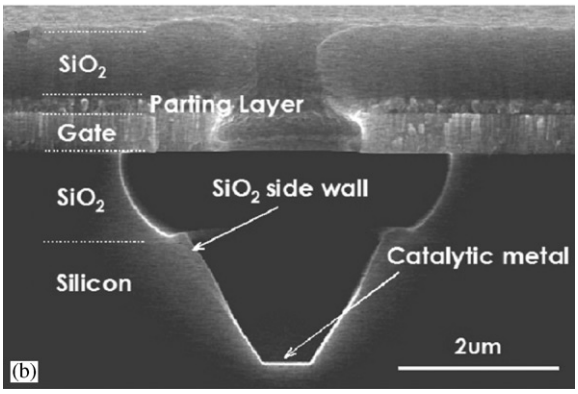


Fig. 2. (a) Schematic diagram for simply fabricating sidewall protector without breaking vacuum, and (b) cross-sectional view of fabricated nanotube emitter just before removing the parting layer.

protector, silicon oxide layer, was deposited by electron beam evaporation during the deposition the substrate was rotated and tilted about an axis perpendicular to the substrate surface. The tilting angles were 15°, 90°, 45°, respectively. Catalytic metal deposited on sidewall was fully covered by insulator layer as shown in Fig. 2(b). Thickness of insulator gradually increases from lower part and the thickness of upper part is about 130 nm. The thickness, position, and depth of sidewall protector could be changed by variation of tilt. After removing parting later, nanotubes were selectively grown in microholes.

Fig. 3(a) shows the SEM image of microgated nanotubes FEA with sidewall protector. Gate aperture is 2 μm in diameter and hole depth is about 2.5 μm. The thickness of gate insulator is 1 μm. Nanotubes are well-aligned perpendicular to the substrate drastically. Fig. 3(b) shows the magnified image of sidewall corresponding to Fig. 3(a). We did not observe nanotubes grown on sidewall having contact with insulator and gate.

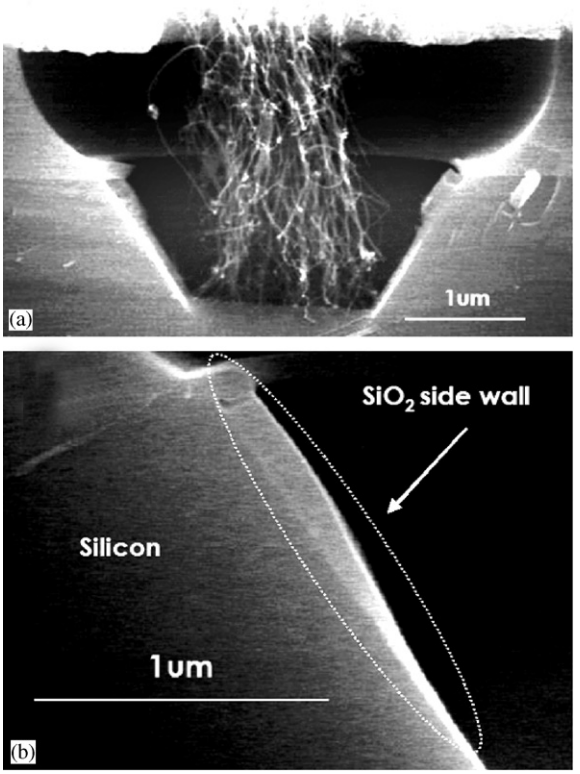


Fig. 3. (a) The SEM image of the microgated emitter using CNTs grown into silicon trench wells with a sidewall protector, and (b) magnified image of sidewall protector after growth of nanotubes.

Emission characterization was carried out in a high vacuum chamber (base pressure 10^{-7} Torr) quipped with cathode, gate, and anode probes. The anode plate was placed about 1 mm from gate metal and anode voltage of 800 V was used. Fig. 4 shows the current–gate voltage characteristics of microgated nanotubes FEA. The nanotubes FEA exhibited a turn-on voltage of 52 V The anode current and gate current are 1.7 and 0.66 μA at a gate voltage of 100 V, respectively. The gate to the anode current ratio, I_g/I_a, was 0.38 at a gate voltage of 100 V. This value is considerably lower than the compared with gate current of microgated nanotubes FEA in our previous report. The Fowler–Nordheim plot of the anode current suggests well-behaved field emission by its high linearity as shown in the inset of Fig. 4.

Fig. 5 reveals the stability of the emission current. There was little degradation of emission current and however, no arcing in the beginning stage. After the short-term aging, the fluctuation was about ±10% over 2600 s when gate voltage was set at 75 V.

In summary, we fabricated microgated nanotubes FEAs using nanotubes directly grown on the substrate by the thermal CVD method. In order to reduce the leakage current due to flowing current

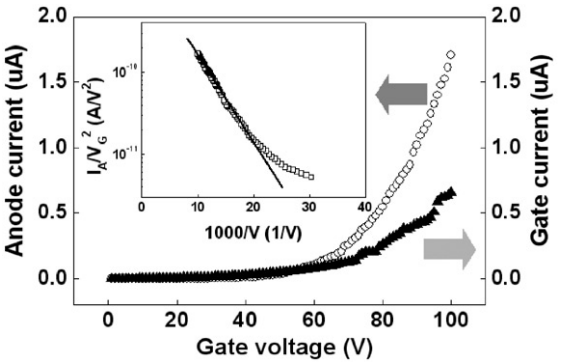


Fig. 4. Field emission current vs. gate voltage, with anode was set at 800 V. The inset is F–N plot of fabricated device.

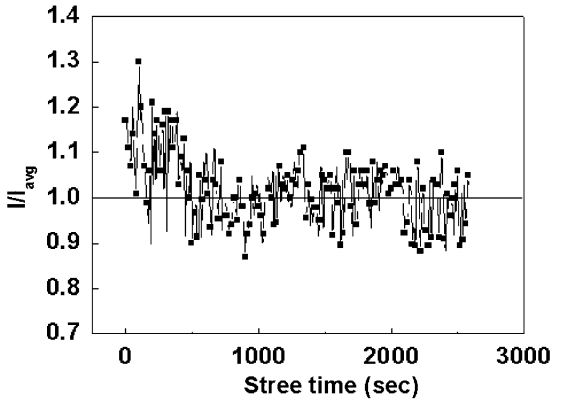


Fig. 5. The current fluctuation vs. stress time as the gate voltage is set at 75 V.

along nanotubes grown on the sidewalls of the gate hole, we adopted very simple processing steps for fabrication of sidewall protector. The field emission properties imply a turn-on gate voltage of 52 V and an emission current of 1.7 μA at 100 V. The sidewall protector has an effect on reducing gate current by suppressing the growth of nanotubes on sidewall. The emission current fluctuation was $\pm 10\%$ over 2600 s. Although there are still a few technical problems to be solved, a microgated FEA with nanotubes directly grown on the substrate is very promising for vacuum microelectronic devices.

Acknowledgements

This work was partially supported by the Information Technology Research Center Program of Ministry of Information and Communication in Korea and by the Intelligent Microsystem Center, which carries out one of the 21st century's Frontier R&D Projects sponsored by the Korea Ministry of Science & Technology (MS-01-325-01).

References

[1] S. Iijima, Nature 354 (1991) 56.
[2] S. Iijima, T. Ichihashi, Nature 363 (1993) 606.
[3] O. Kuttel, et al., Appl. Phys. Lett. 73 (1998) 2113.
[4] J.-M. Bonard, J.-P. Salvetat, T. Stockli, L. Forro, A. Chatelain, Electrochemical Society Proceedings Col. 98–8, 1998, p. 783.
[5] A.A. Talin, B.F. Coll, Y. Wei, K.A. Dean, J.E. Jaskie, Electrochemical Society Proceeding, 2000, p. 247.
[6] S.D. Ahn, Y.H. Song, S.Y. Choi, J.B. Park, J.I. Shon, S.H. Lee, J.H. Lee, K.I. Cho, Proceedings of the 14th International IEEE Vacuum Miccroelectronics Conference, 2001, p. 31.
[7] K.J. Chen, W.K. Hong, C.P. Lin, K.H. Chen, L.C. Chen, H.C. Cheng, IEEE Electron. Dev. Lett. 22 (2001) 516.
[8] G. Pirio, P. Legagneux, D. Pribat, K.B.K. Teo, M. Chhowalla, G.A.J. Amaratunga, W.I. Milne, Nanotechnology 13 (2002) 1.
[9] Y.H. Lee, Y.T. Jang, D.H. Kim, J.H. Ahn, B.K. Ju, Adv. Mater. 13 (2001) 479.
[10] Y.T. Jang, C.H. Choi, B.K. Ju, Y.H. Lee, M.H. Oh, N.K. Min, J.H. Ahn, Society for Information Displays, International Symposium Digest of Technical Papers, 2002, p. 377.
[11] David S.Y.Hsu Hsu, Appl. Phys. Lett. 80 (2002) 2988.
[12] C.A. Spindt, C.E. Holland, A. Rosengreen, Ivor Brodie, IEEE Trans. Electron. Dev. 38 (1991) 2355.
[13] C.A. Spindt, L. Ivor Brodie, E.R. Humphrey, Westerberg, J. Appl. Phys. 47 (1976) 248.