Co-doped TiO_2 nanowire electric field-effect transistors fabricated by suspended molecular template method

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We report on the fabrication of Co 3.4 at. % doped TiO_2 nanowire-based field-effect transistors with a back gate of heavily doped Si substrate and their electric field-effect functions. The TiO_2:Co nanowire, which was fabricated utilizing a conventional magnetron sputtering technique on a suspended molecular template between electrodes, is a polycrystalline and consists of a chain of nanoparticles on a molecular template. The *N*-type field-effect transistors prepared from the suspended Co–TiO_2 nanowire junction were exhibited on currents, transconductances, and a mobility of up to 0.1 mA/μm, 0.2 μA/V, and $\mu_e \approx 66$ cm^2/V s, respectively, at room temperature. The unique structure of these inorganic-organic functional devices may enable the fabrication of flexible nanoelectrospin devices. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1851614]

Nanoelectronics, based on nanotubes and nanowires, is considered one of the most promising alternative solutions to breaking the scaling limit of silicon-based integrated devices. Recently, various kinds of nanowires were successfully synthesized and tailored to work as interesting nanoelectronics: building blocks such as nanoscale transistors, displays, self-generated light-emitting diodes, and chemical and bio sensors.[1–4] On the other hand, intensive interest in spintronics has made it possible to study such materials as the diluted magnetic semiconductor (DMS). Among the DMS materials, Co-included TiO_2 thin films have received a lot of attention because of their possible practical applications in spintronics, though the nature of the ferromagnetism is still arguable.[5–8] To take a step forward and explore the role of DMS in future teralevel integrated nano-magneto electronics, it is important to provide a fabrication of low-dimensional nanowires. A few successful approaches to the fabrication of Mn-doped ZnO nanowire or Co-doped TiO_2 nanotapes of complex materials, such as ternary and quaternary systems, were reported with basic magnetisms for large bundles of synthesized nanomaterials.[9–13] The combination of the physical properties of the Co–TiO_2 system with the fabrication of nanotechnology makes this material a promising candidate in providing nano-electronic devices. It is, therefore, very crucial to study gate-voltage-controlled functionalities for their specific applications as real nanodevices.

In this regard, we report an approach to the fabrication of Co-doped TiO_2(Co-TiO_2) nanowires and the electric field-effect-transistor (FET) function of Co-doped TiO_2 nanowires. In our process, flexible organic poly (3,4-ethylenedioxythiophene) (PEDOT) nanowires, which we synthesized,[14] were used as suspended templates for the growth of sputter-coated Co-doped TiO_2 nanowires. A suspended templating technique[15,16] results in Co-doped TiO_2 nanowires, which are thinner than 200 nm in diameter. First, conducting 100-nm-thick PEDOT nanotubes were synthesized using an electrochemical polymerization method with an Al_2O_3 nanoporous ($D \approx 200$ nm) template purchased from Whatman Co. For the electrical study, drain and source electrodes were defined using photolithography after the dispersion of the PEDOT as a template on the patterned substrate. Here, the pre-patterned Nb films were used as coordinate markers in searching for the position to make contact with the Co–TiO_2 nanowires. Then, the metallic wiring was done after confirming the position of dispersed nanowires. Here, all of the contact electrodes and Co-doped TiO_2 wires were fabricated using a conventional reactive radio frequency magnetron sputtering technique. The nanometer-thick Co–TiO_2 ($\sim$50 nm) was deposited on a molecular bridge, acting as a template, through reactive sputtering. This method utilized a mixture of Ar(70%)+O_2(30%) gases with 8 wt% Co-doped TiO_2 ceramic target (purity 99.99%) under a vacuum pressure of 5 mTorr at 300 °C. Finally, we obtained Nb-nanowire-Nb junctions using a degenerately doped Si back gate in a controllable manner.

The fabricated PEDOT nanowires, Co–TiO_2 nanowire bundles, and a fabricated transistor are shown in Figs. 1(a) and 1(b), respectively. The Co–TiO_2 bulk, which was deposited through a conventional magnetron sputtering method, was nearly stoichiometric with about 4 at. % of Co. This was determined through in-depth profiling with Auger electron spectroscopy (not shown in this letter). An energy dispersive spectroscopy (EDS) on the Co–TiO_2 performed onto the PEDOT using high resolution tunneling electron microscopy (Jeol 2010) shows the presence of Ti, O, and a trace of Co. The compositional analysis data show that Ti:O:Co $\sim$30.6:66.0:3.4 as displayed in Fig. 1(c). The topology of the examined nanowires indicates that the nanowires consisted of nanobead-like structures across the whole length of the fiber. In both cases of reactively sputtered TiO_2 films[16] and nanowires[11–13] the low surface mobility caused by the high gas pressure and the low substrate temperatures of 300 °C produced a structure consisting of low density and

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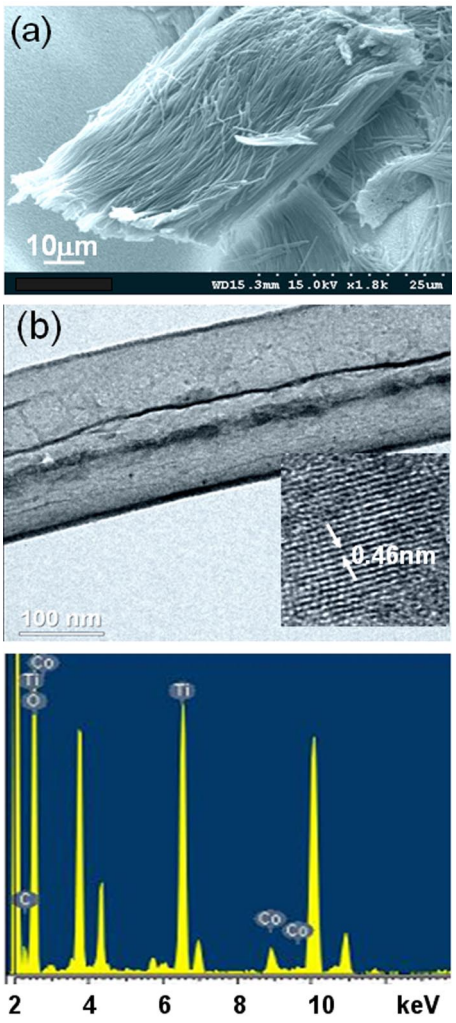

FIG. 1. (Color online) The fabricated Co-doped TiO_2 nanowire by suspended templated method. (a) Suspended PEDOT nanowires as a template, (b) transmission electron microscopy images of the Co-doped nanowire bundles and enlarged portion near the surface of a Co–TiO_2 wire, (c) EDS spectrum of Co–TiO_2 nanowire showing characteristic peaks for Co and Ti. The atomic percent is about Ti:O:Co~30.6:66.0:3.4 as an average value of several measurements.

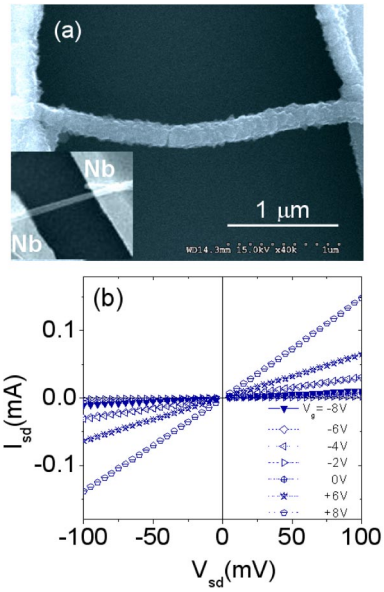

FIG. 2. (Color online) (a) A suspended Co–TiO_2 nanowire junction between Nb electrodes. Inset figure represents the suspended molecular template junction before fabrication of Co–TiO_2 nanowire. (b) Room temperature channel current (I_{sd}) vs drain-source (V_{sd}) voltage characteristics. In the low bias regime the figure shows that the device has ohmic contact properties with relatively high current levels.

surface texture, such as a roughened and evenly granulated surface. Previous reports on the formation of metal nanowires on carbon nanotubes have revealed that the weak interaction between the deposited material and the template together with the high diffusion rates lead to fewer nucleation sites for crystal growth and large particle formation.[15] The most frequent diameter of nanowires was about 100 nm. It depended, though, on the diameter of the molecular template PEDOT. A typical image of nanowires individually suspended between electrodes is shown in Fig. 2(a). The figure shows that it is clear that the nanowire consisted of randomly stacked grains.

Electrical transport measurements were conducted to evaluate the performance of our TiO_2 nanowires fabricated using the suspended molecular template method. Measurements were taken using the two probes of the Nb source and the drain contacts whose typical separation was 2 μm on the top channel configuration, and gated via the degenerately doped Si substrate through a SiO_2 gate insulator. In this study, all the electronic measurements were conducted at room temperature using a semiconductor characterization system (Keithley 4200) with equipped preamplifiers. In order to screen the 27 specimens more effectively, we used a probe station (Cascade Co.) with the Pt probe. In all our measurements, V_{sd} and V_g were applied with respect to the grounded source contact and were acquired at room temperature under ambient humidity.[17] The linear relationship of the I_{sd} and V_{sd} at a low drain-source bias indicates the formation of a good ohmic contact to the nanowire. The figure shows that a negative gate bias reduces the current, while a positive V_G increases the current. Thus, the device behaves as an *n*-channel FET since the increase of the channel current (I_{sd}) at a positive gate voltage is characteristic of an *n*-channel field effect transistor (FET). We prepared 27 devices for FET fabrication and although not all of them demonstrated the same combination of characteristics, almost all of the tested devices showed a semiconducting behavior. The device shown in Fig. 2(a) can carry a current of up to 0.15 mA in its "on state." Figure 2(b) shows typical channel current (I_{sd}) versus drain-source bias voltage (V_{sd}) (output characteristics) characteristics at different values of the gate voltage (V_g) for the typical three-terminal nanowire junction. In the following, however, we focused on devices with bad contacts, which are more typical of our work. Figure 3(a) illustrates the output I_{sd}-V_{sd} characteristics of bad contact devices. When the V_{sd} is increased from 0 using constant V_g, the V_{sd} differential conductance gradually decreases until the current saturation takes place. After this [see Fig. 3(b)], when increasing the drain-to-source bias under constant V_g the differential conductance gradually decreases and the observed channel current begins to saturate. Considering the fact that this kind of current saturation for an applied V_{sd}, which is greater than the pinch-off V_{sd}, would be observed in a FET with very large channel length and our geometrical channel length is only about 2 m, we interpret the results as the effective channel length was assumed to be a constant, independent of V_{sd} and the resistance of the channel remained practically constant with the increasing V_{sd}.

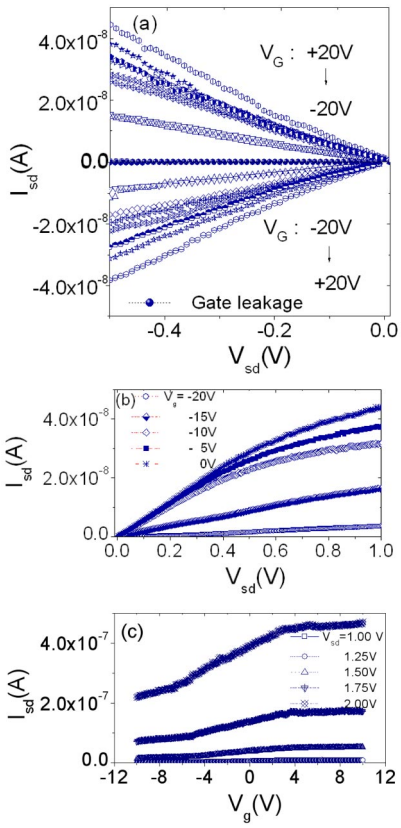

FIG. 3. (Color online) (a) Drain-to-source conduction slightly below saturation as a function of V_g, (b) saturation of the I_{sd} as a function of the V_G for the channel in the region of high bias, and (c) response characteristics (I_{sd} -V_g) of transistors with change of V_{sd}. Typical *n*-channel FET characteristics were shown.

Next, we measured the transfer curves (I_{sd} vs V_g) of the nanowire junctions. The threshold voltage of the rise of conduction (V_{th}) and the transition width were about −5 and 8 V, respectively. The channel on current is two times higher than that of the off current, as displayed in Fig. 3(c). The transconductance characterizing gate bias dependence, which was estimated from the slopes of the I_{sd}-V_g curves, has values of $g_m = \partial I_D / \partial V_G \sim 0.2 \times 10^{-6}(A/V)$. The carrier density and mobility of the *n*-type FET at room temperature, with contact electrodes, can be determined by assuming a homogeneous carrier distribution along the nanowire and the total charge Q on the nanowire as $Q = CV_T$, where C is the device capacitance.[17,18] If we model the nanowire as a metallic cylinder, the device capacitance per unit length, with respect to the back gate, is $C/L \approx 2\pi\varepsilon\varepsilon_0/\ln(2h/r)$, where ε is the dielectric constant of the gate insulator SiO_2, ε_0 is the vacuum dielectric constant, r and L are the nanowire radius and length, respectively, and h is the thickness of the device. L =2000 nm, d=200 nm, h=1000 nm, and $\varepsilon \approx 2.5$ provides a one-dimensional carrier density of $n = Q/eL \approx 1.8 \times 10^{10}$ cm^{-1} for a threshold voltage of $V_T \sim -5$ V. We see that this value of carrier density is very much lower than those of the Fe-doped TiO_2 thin films.[18] Assuming a diffusive transport in our nanowire at room temperature, we estimate the carrier mobility from the transconductance, g_m, of the Co−TiO_2 nanowire FET. Since the carrier mobility is constant in the linear regime of the I_D-V_{SD} curve, we got the mobility $\mu_e \approx 66$ cm^2/V s using $g_m = \partial I_D / \partial V_G = \mu_h C V_{SD}/L^2$ at V_{sd}=1 V. This analysis shows that the value of the gate capacitance is a very important physical parameter in enhancing gate response by increasing the carrier density, as well as the carrier mobility. In other words, the channel current in the OFF state is limited by tunneling through the barrier at the source. It is, therefore, a function of the thickness of the gate insulator. Thus, in order for such templated nanowires to work well, it will be important to study both the high dielectric gate insulator and the magneto-transport behavior of the nanowire under a magnetic field with a gate bias.

To summarize, we have demonstrated the Co−TiO_2 nanowire field-effect transistor using the suspended template method, based on the sputter deposited Co−TiO_2 nanowires and the PEDOT nanowire as substrates. Compared to other recent nanowire-based FETs, the Co-doped TiO_2 exhibits relatively high transconductnace $\sim 0.2 \times 10^{-6}(A/V)$ and a high on current. The unique structure of these inorganic-organic functional devices may contribute to the fabrication of flexible nano-electro-spin devices and provide low-dimensional building blocks for gate-controlled devices, through the magneto-transport behavior of the nanowire with a gate bias under the magnetic field.

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